

Fig.1 (Prior Art)

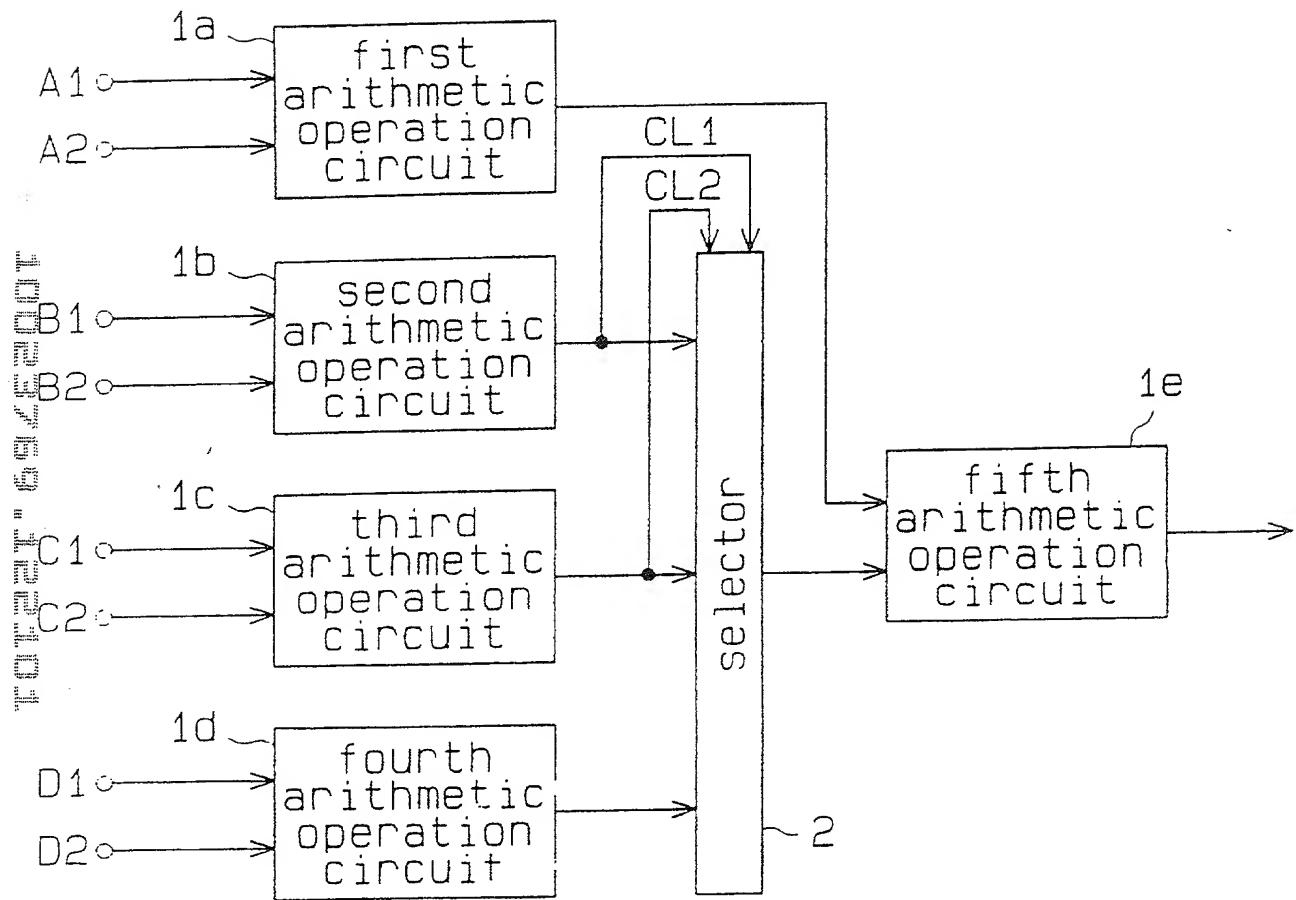


Fig.2

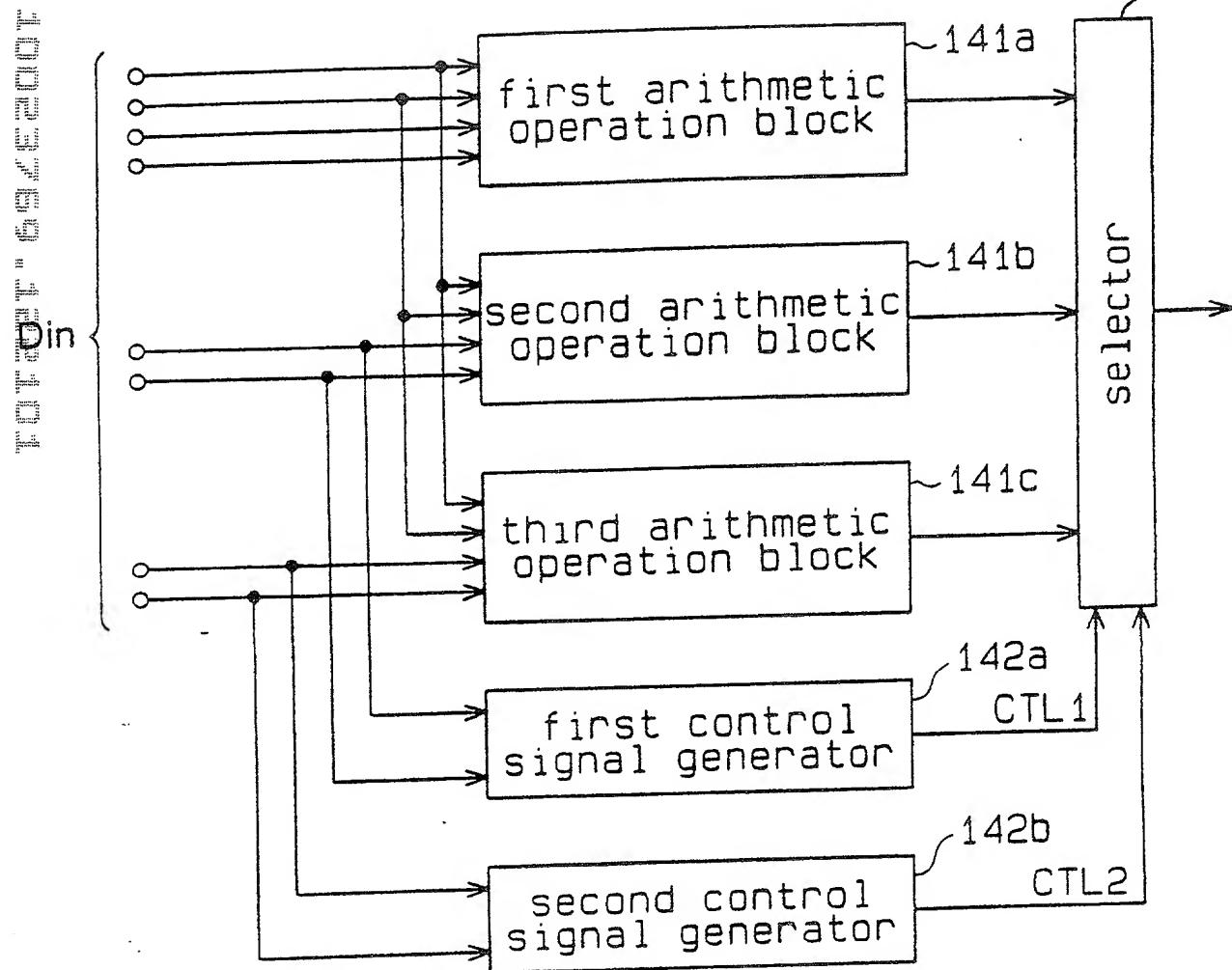


Fig. 3

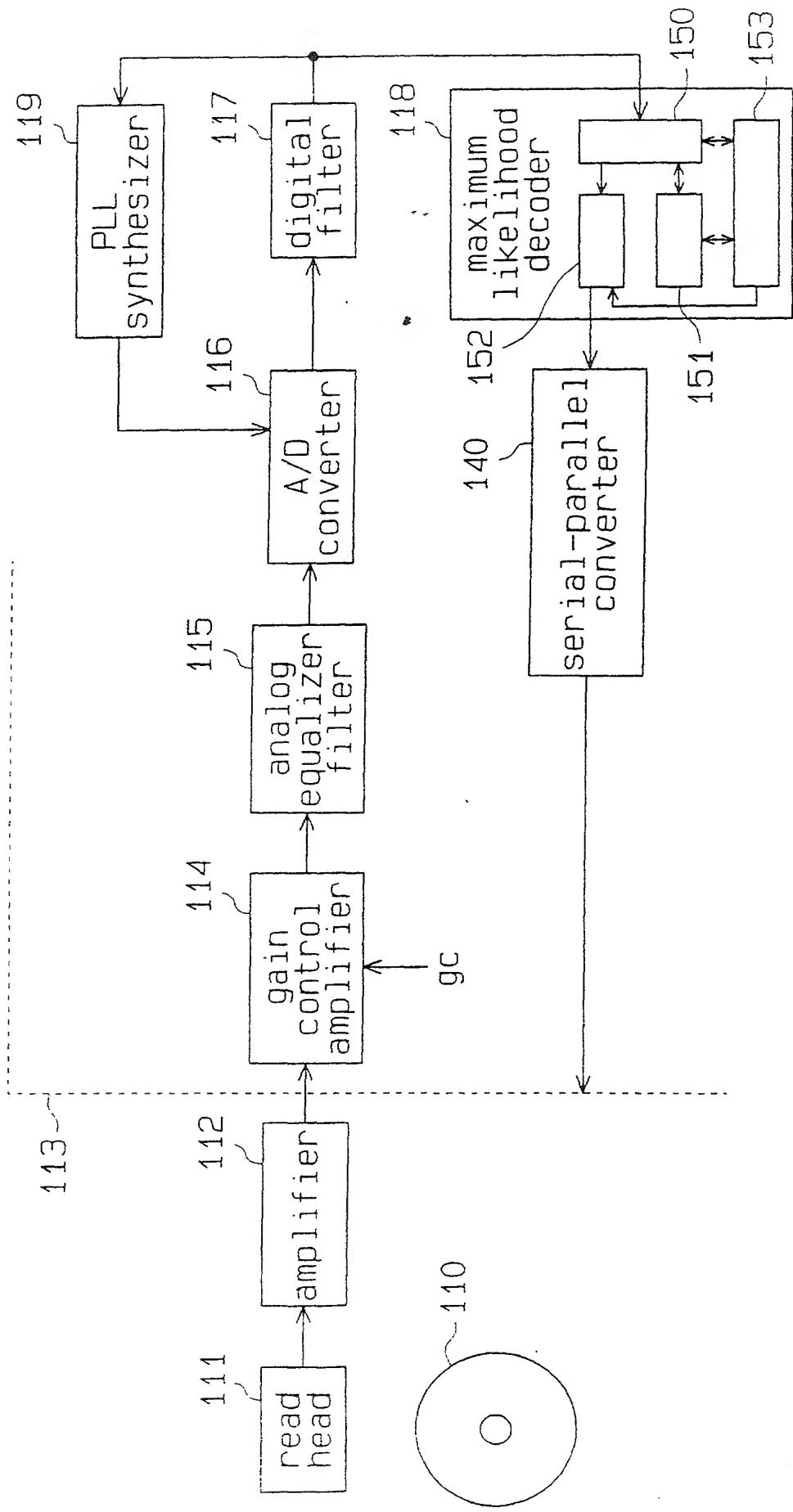


Fig. 4

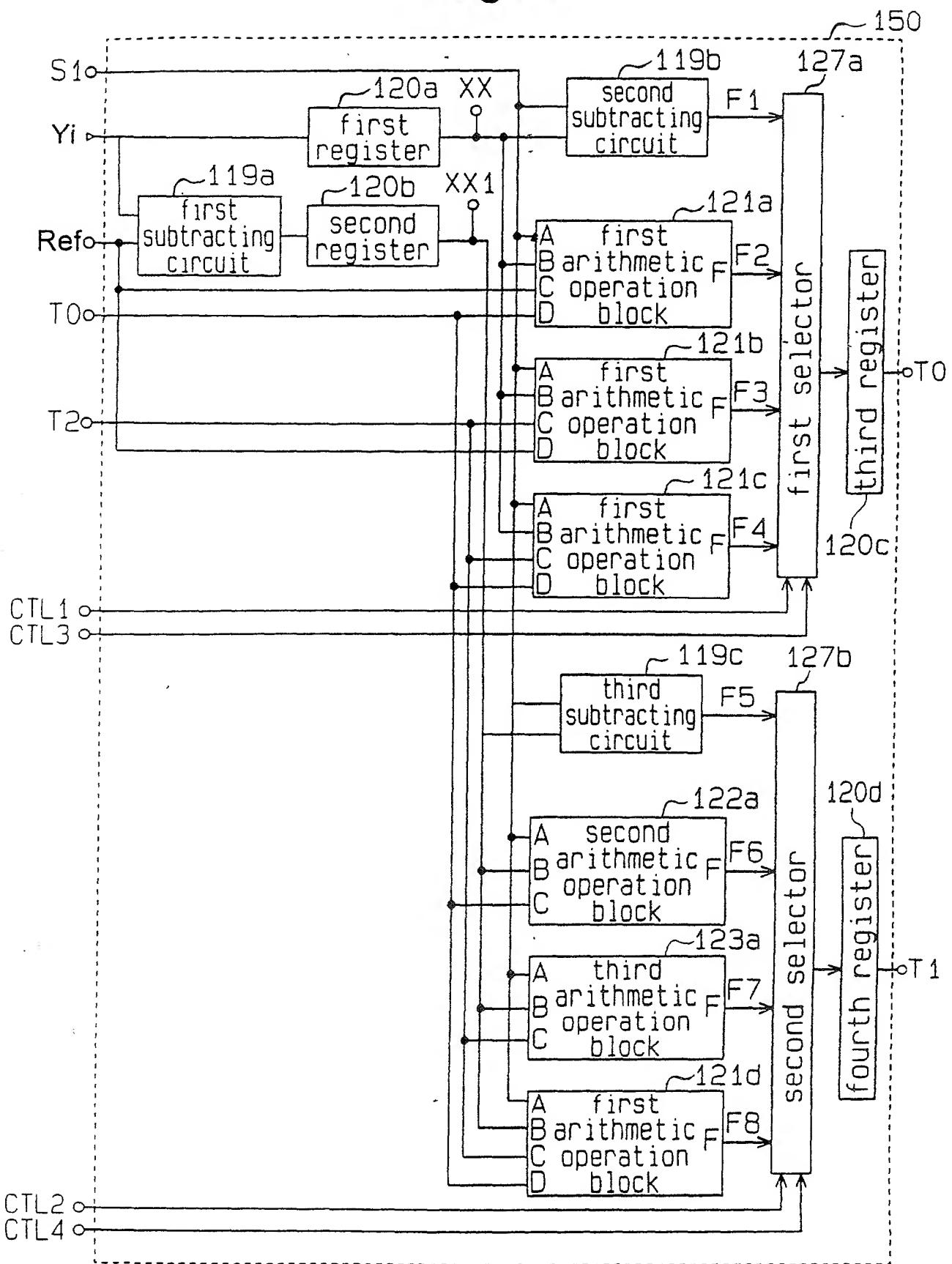


Fig. 5

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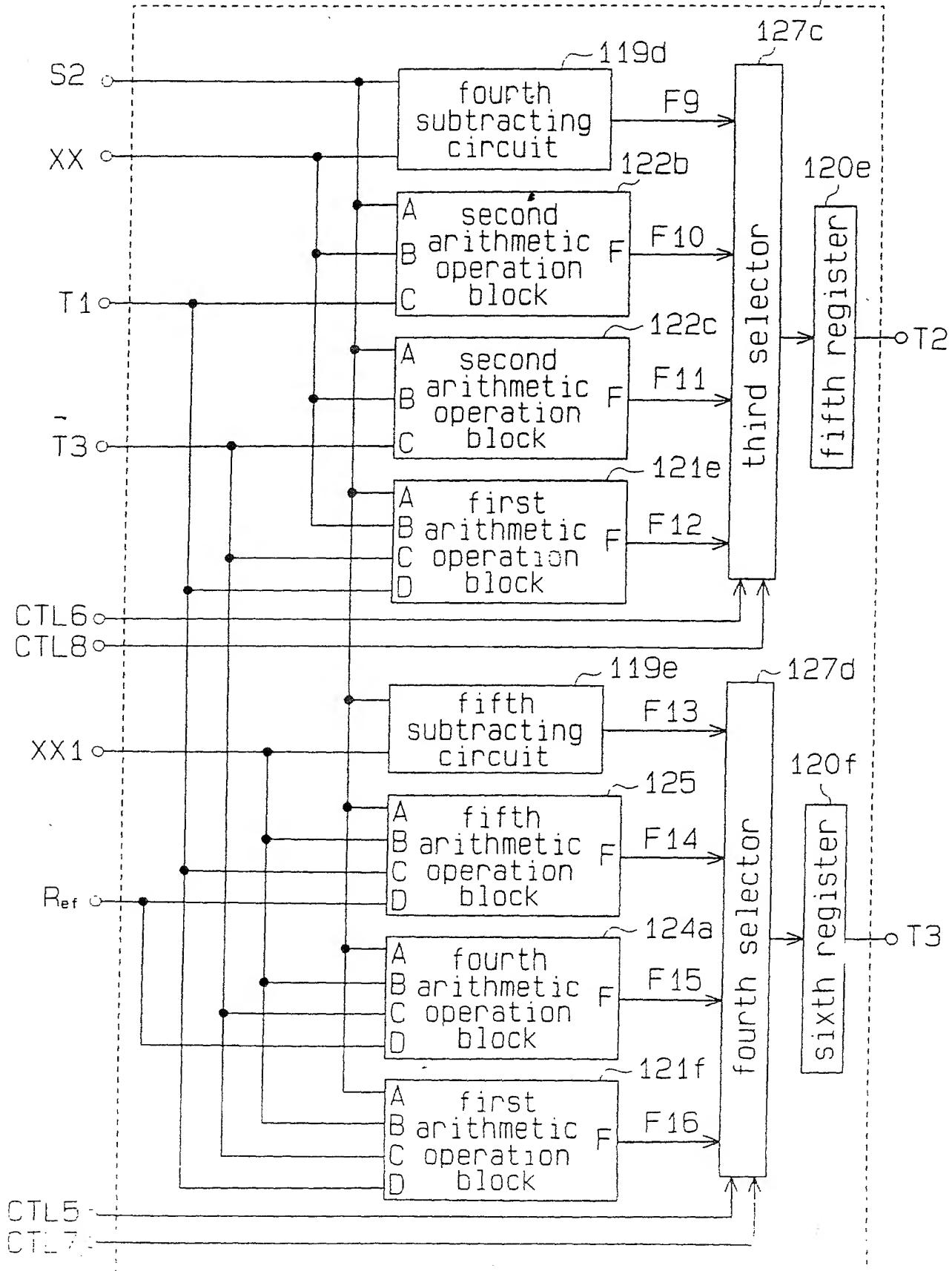


Fig.6

~ 152

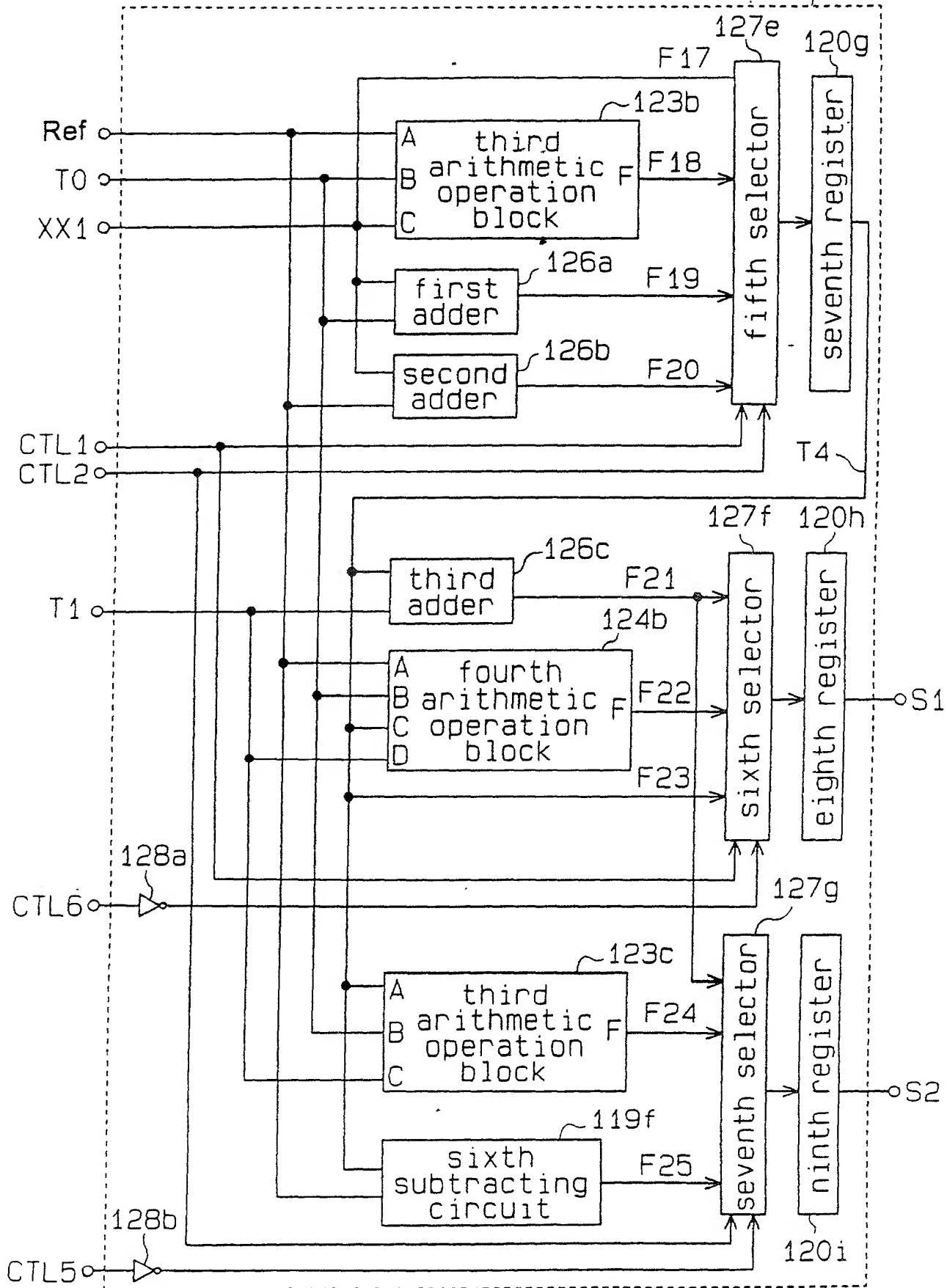


Fig.7

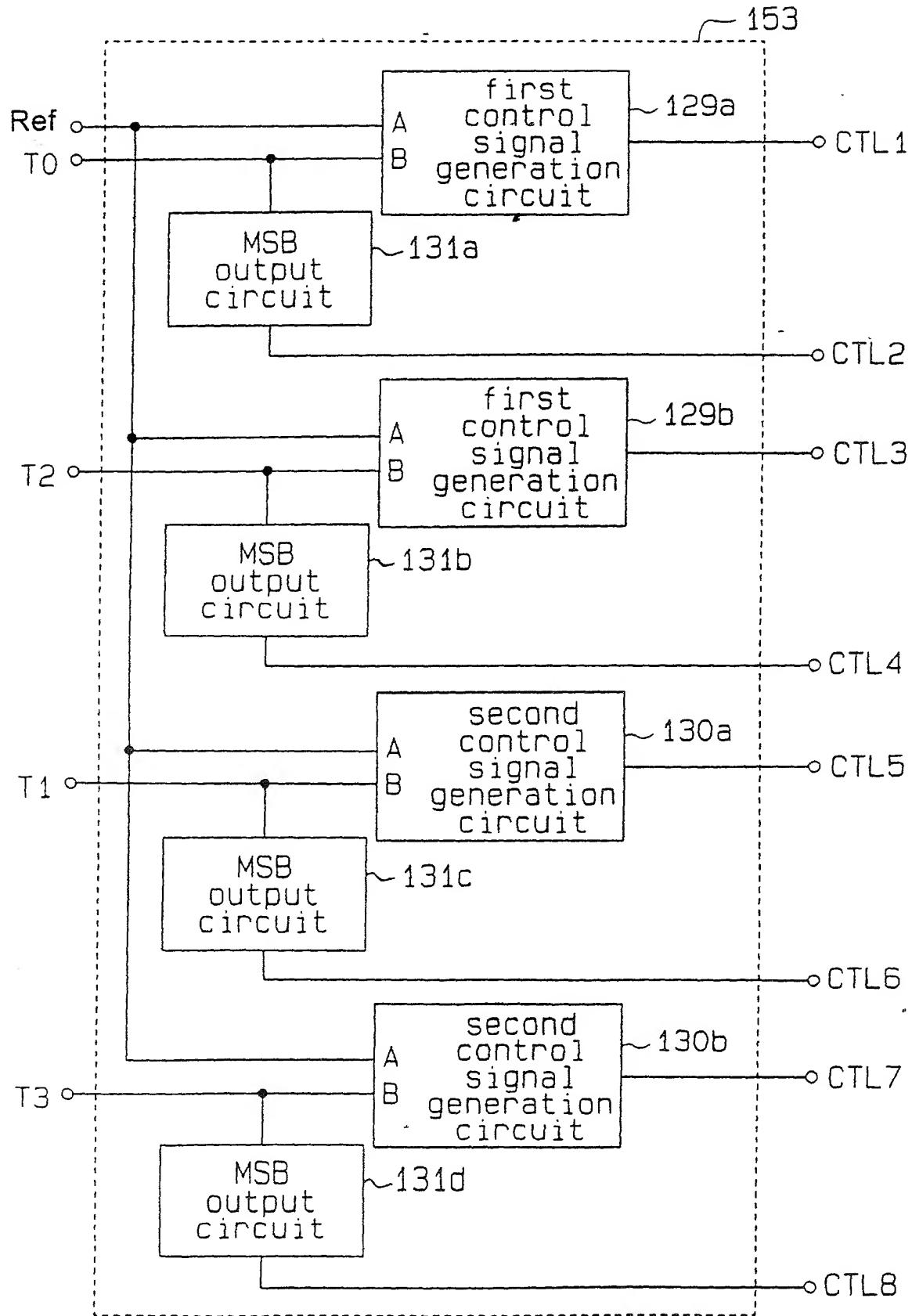
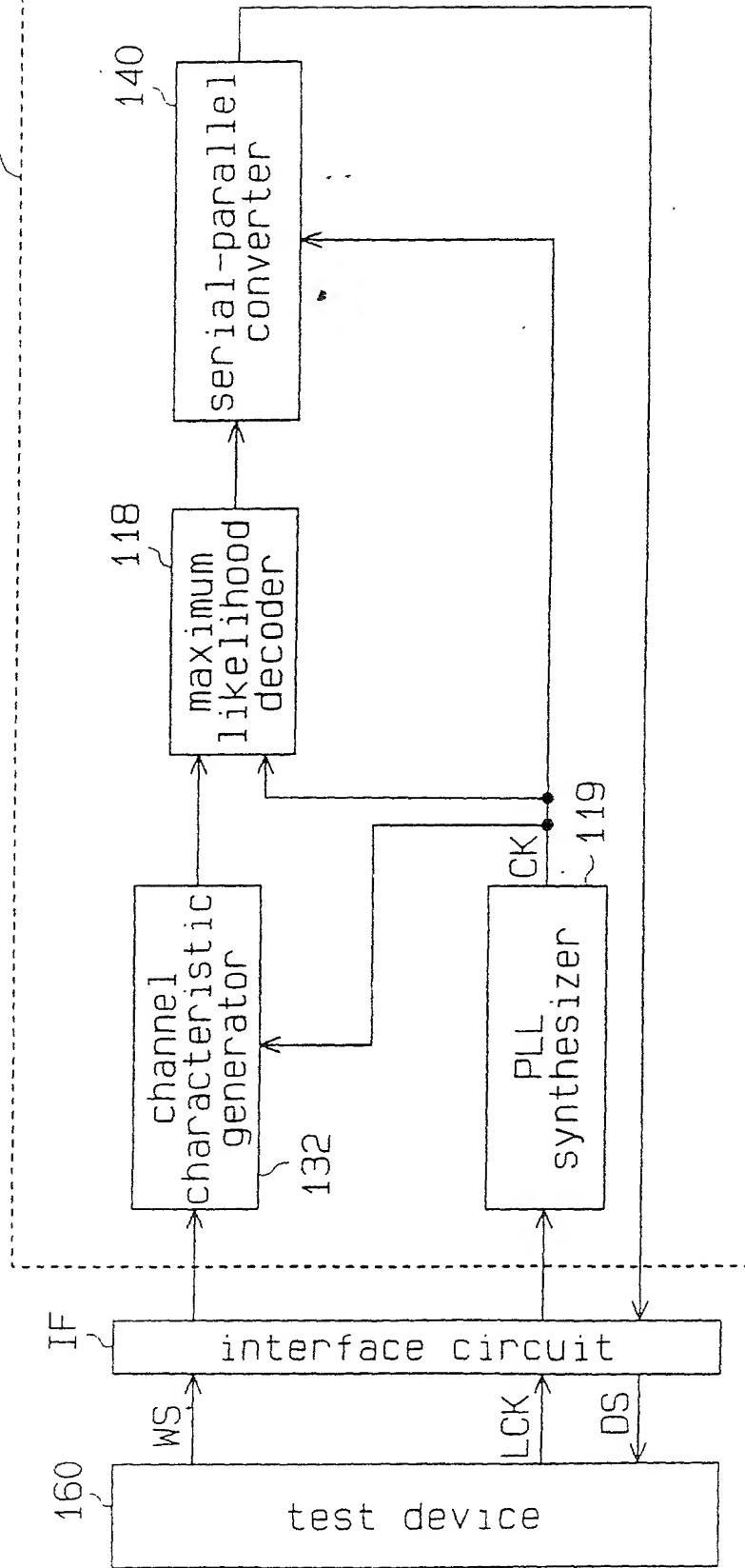


Fig. 8

113



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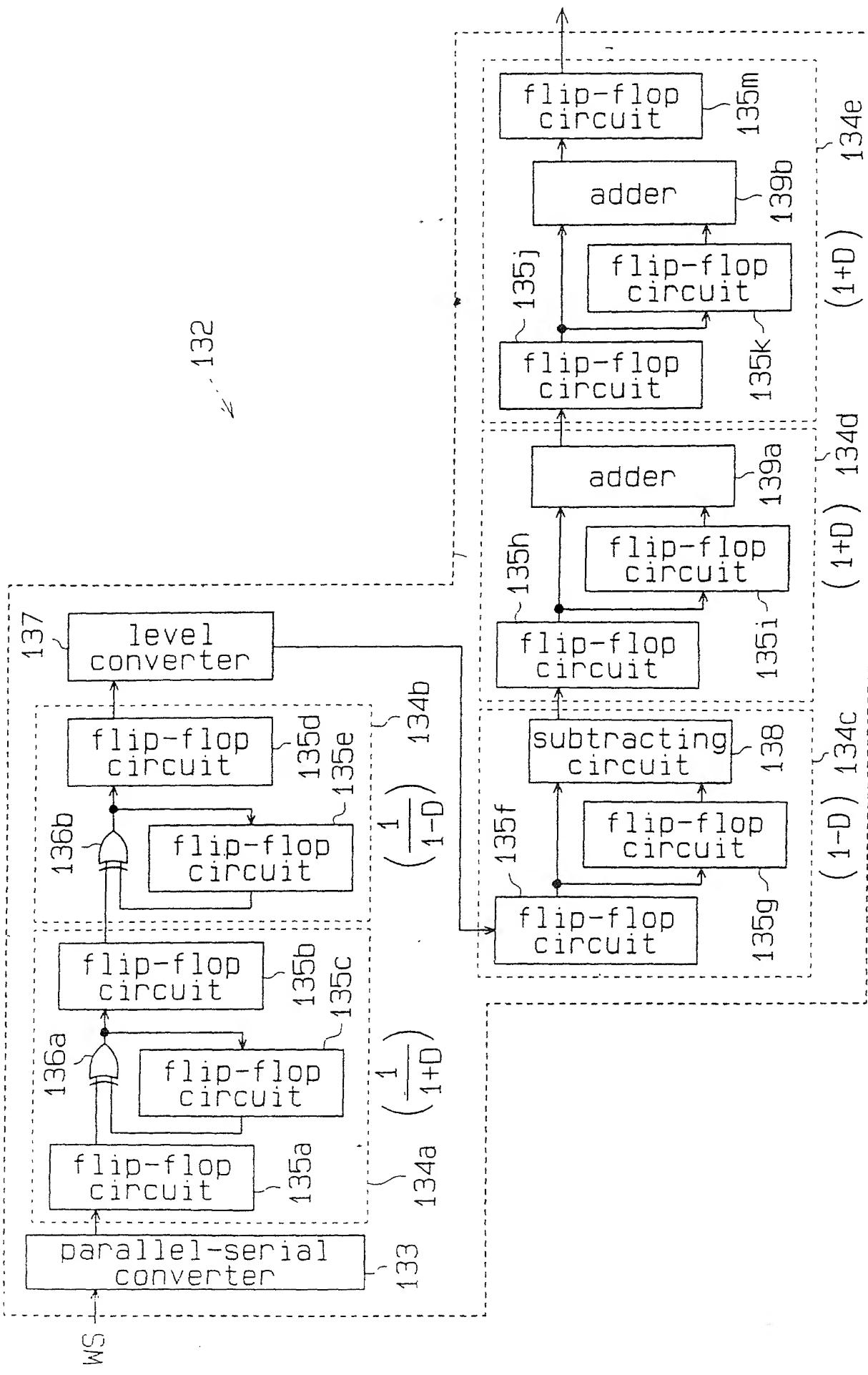


Fig. 10

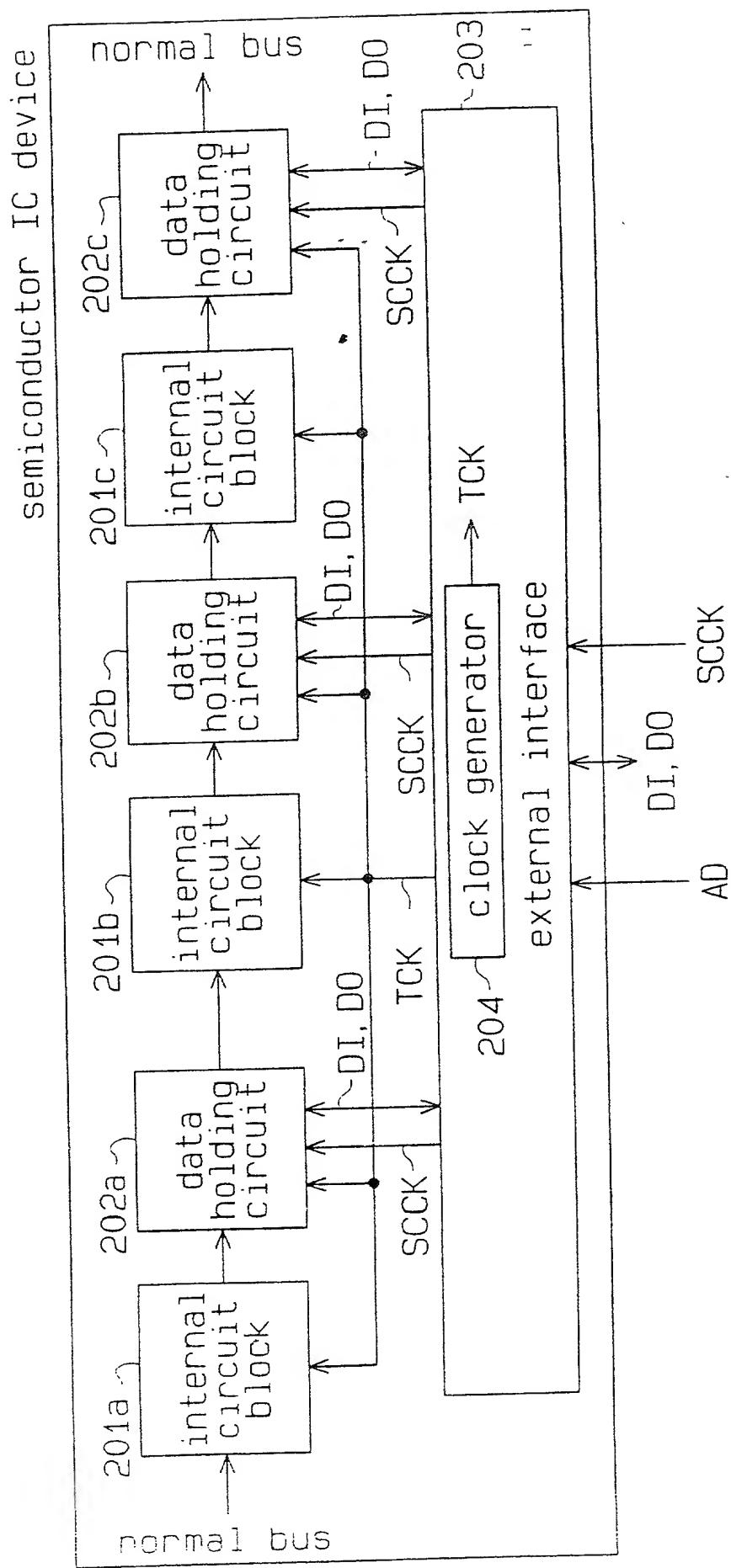


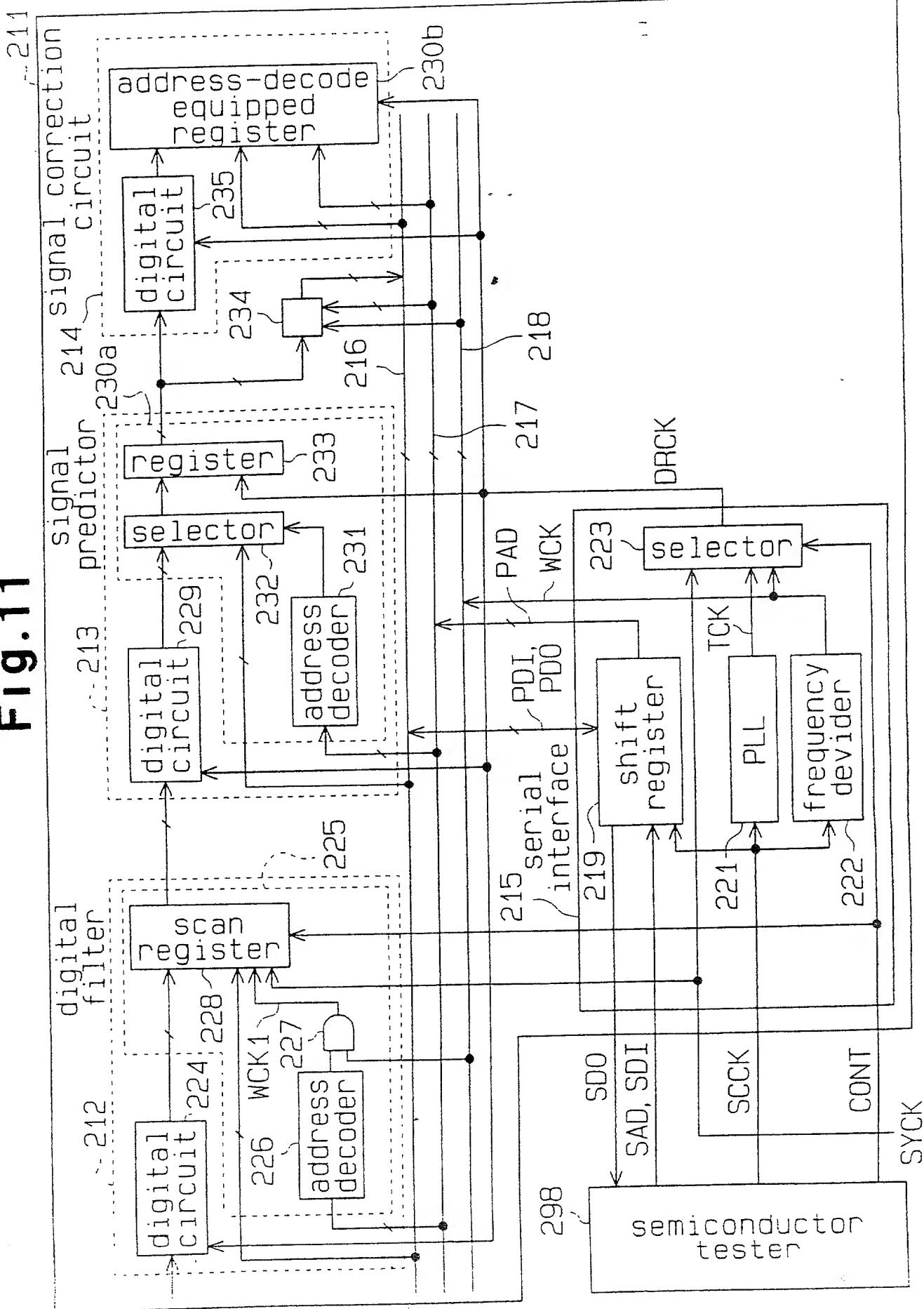
Fig. 11

Fig. 12

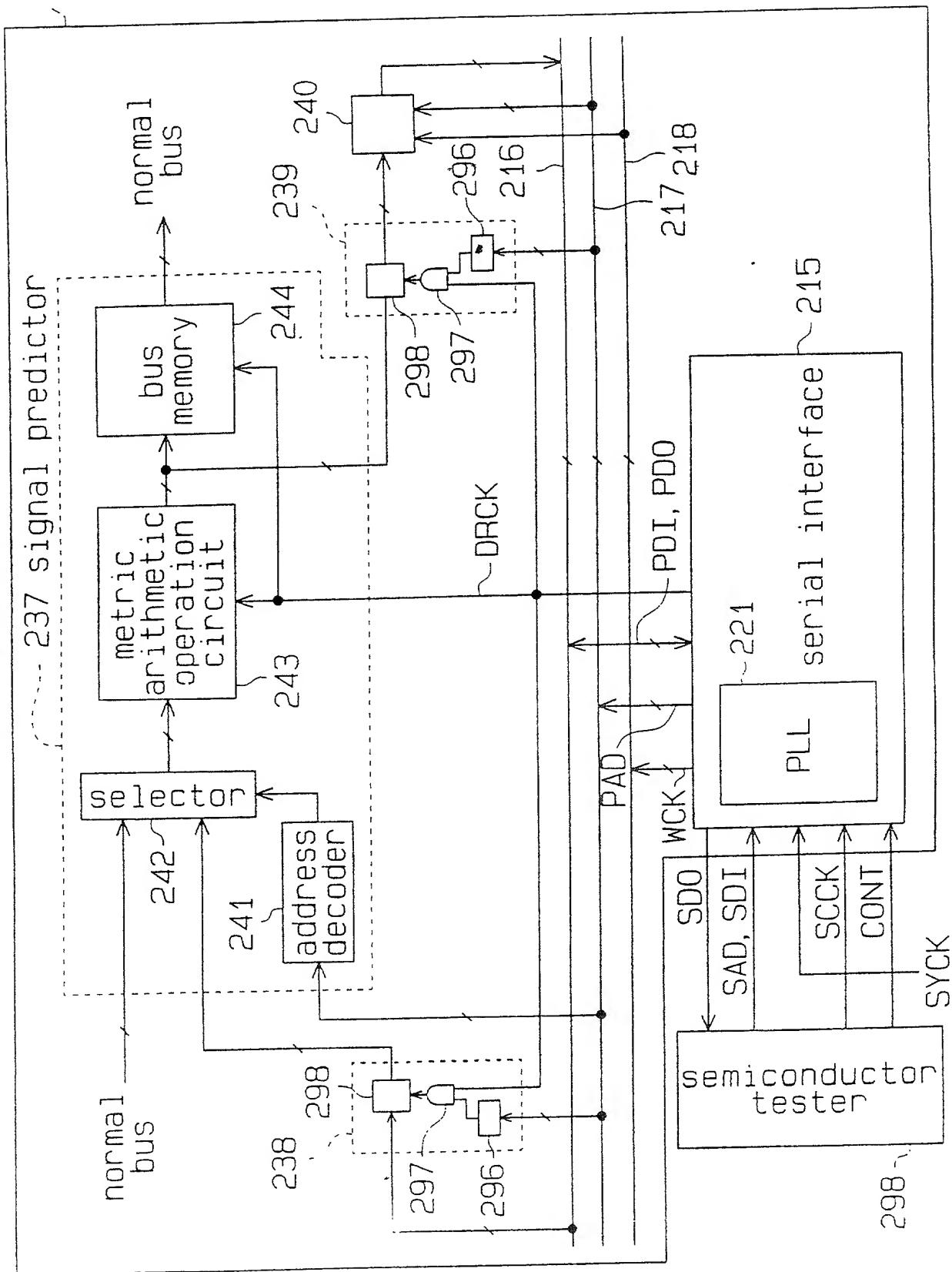


Fig. 13 Схема

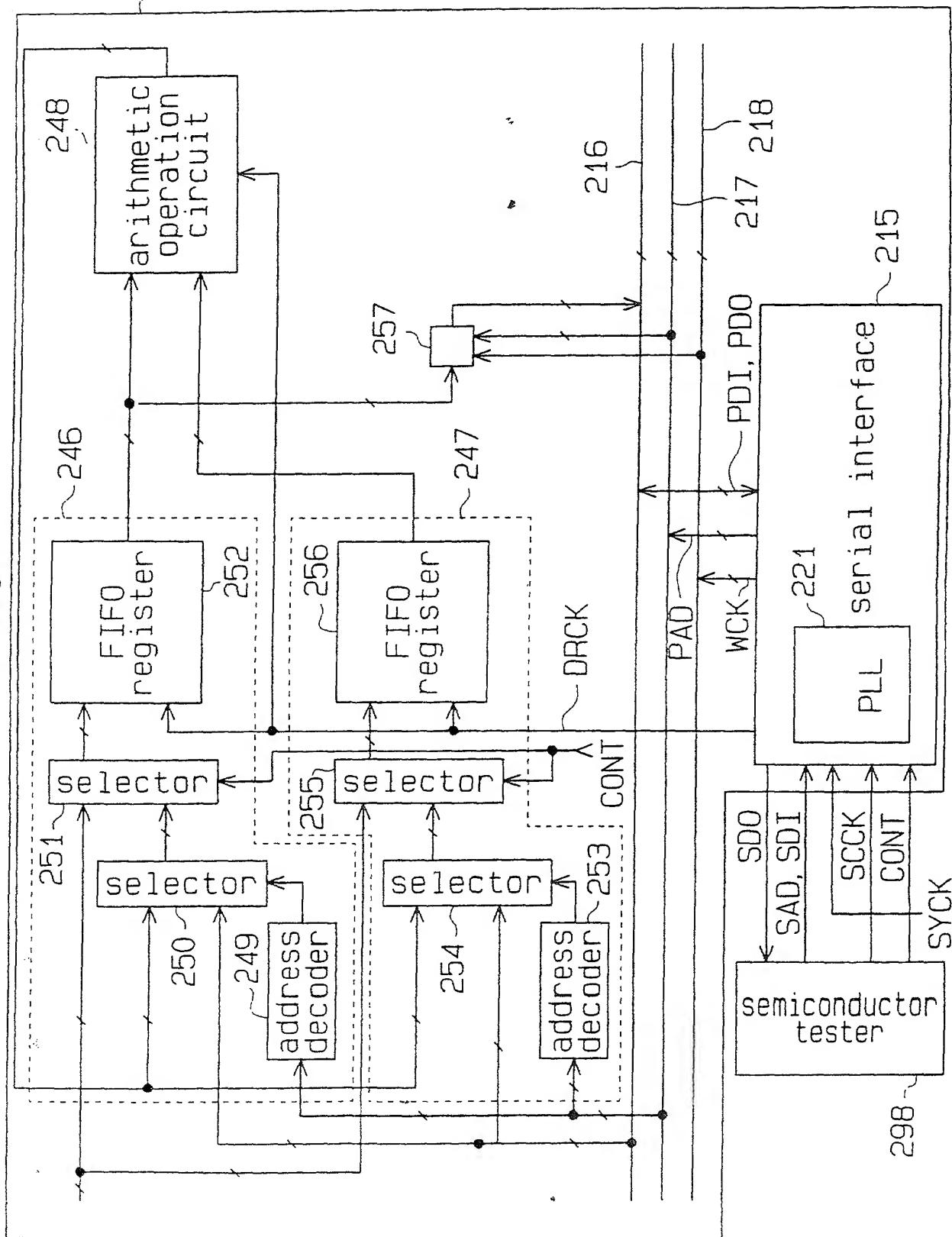


Fig. 14

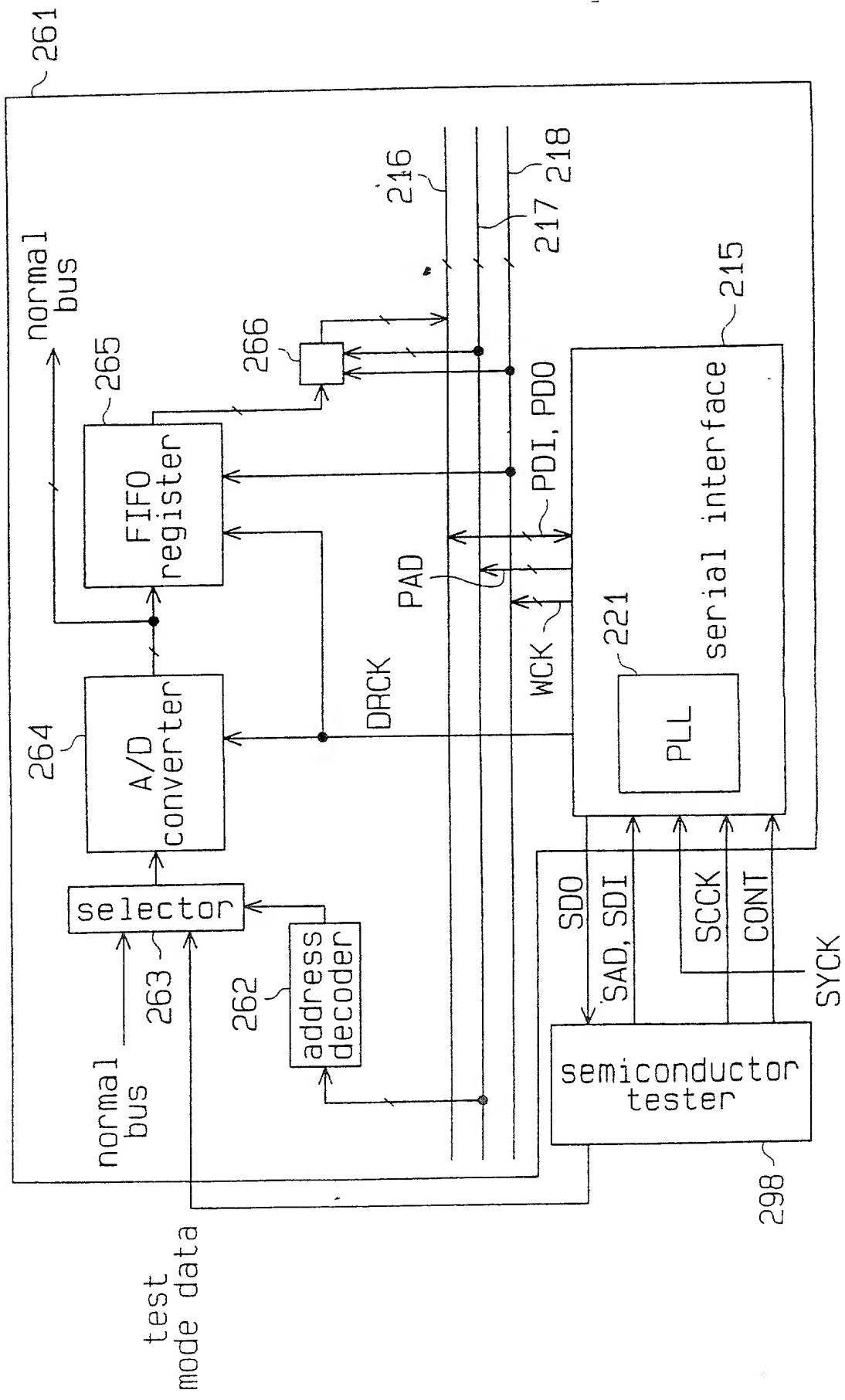
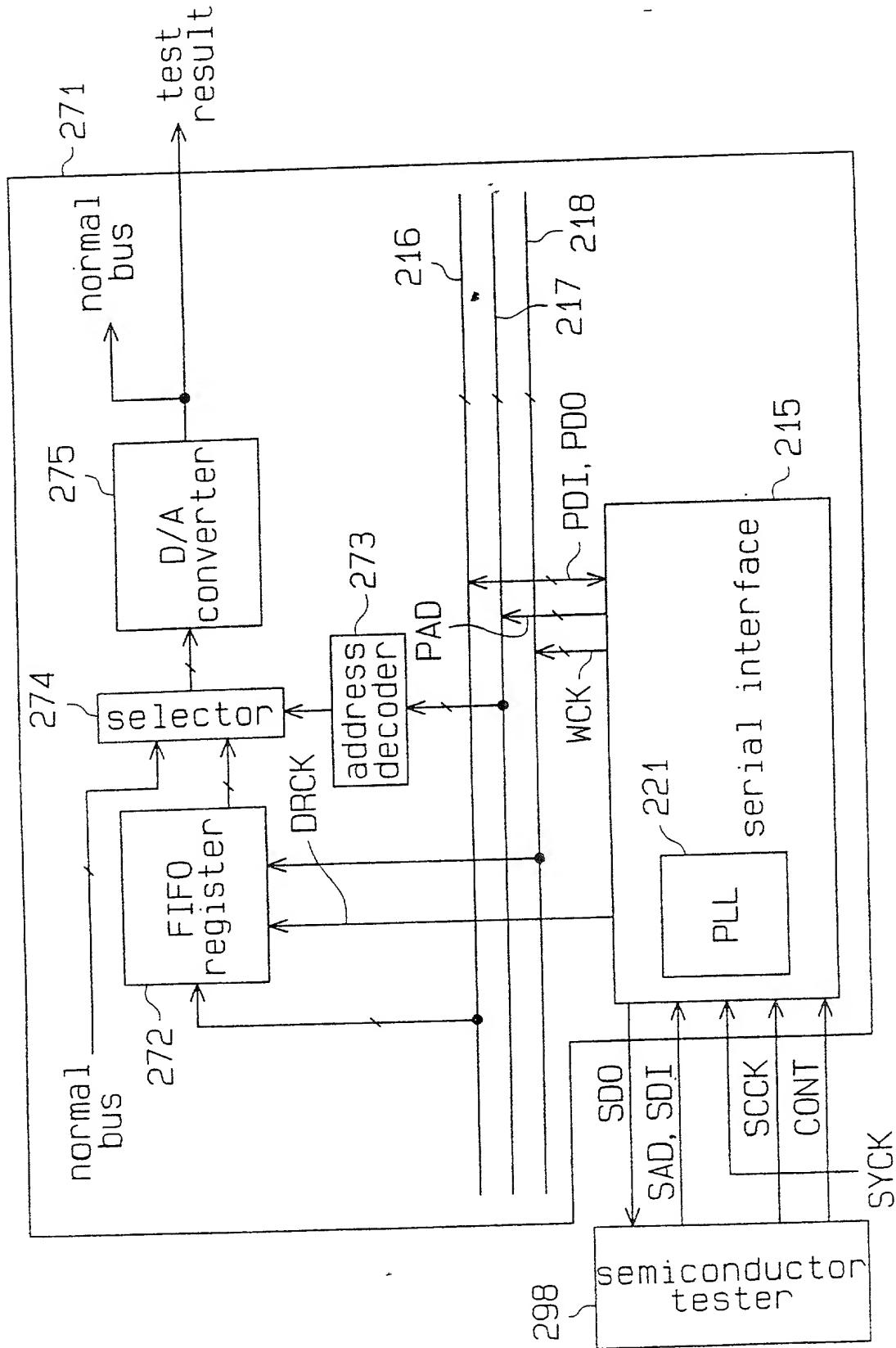


Fig. 15



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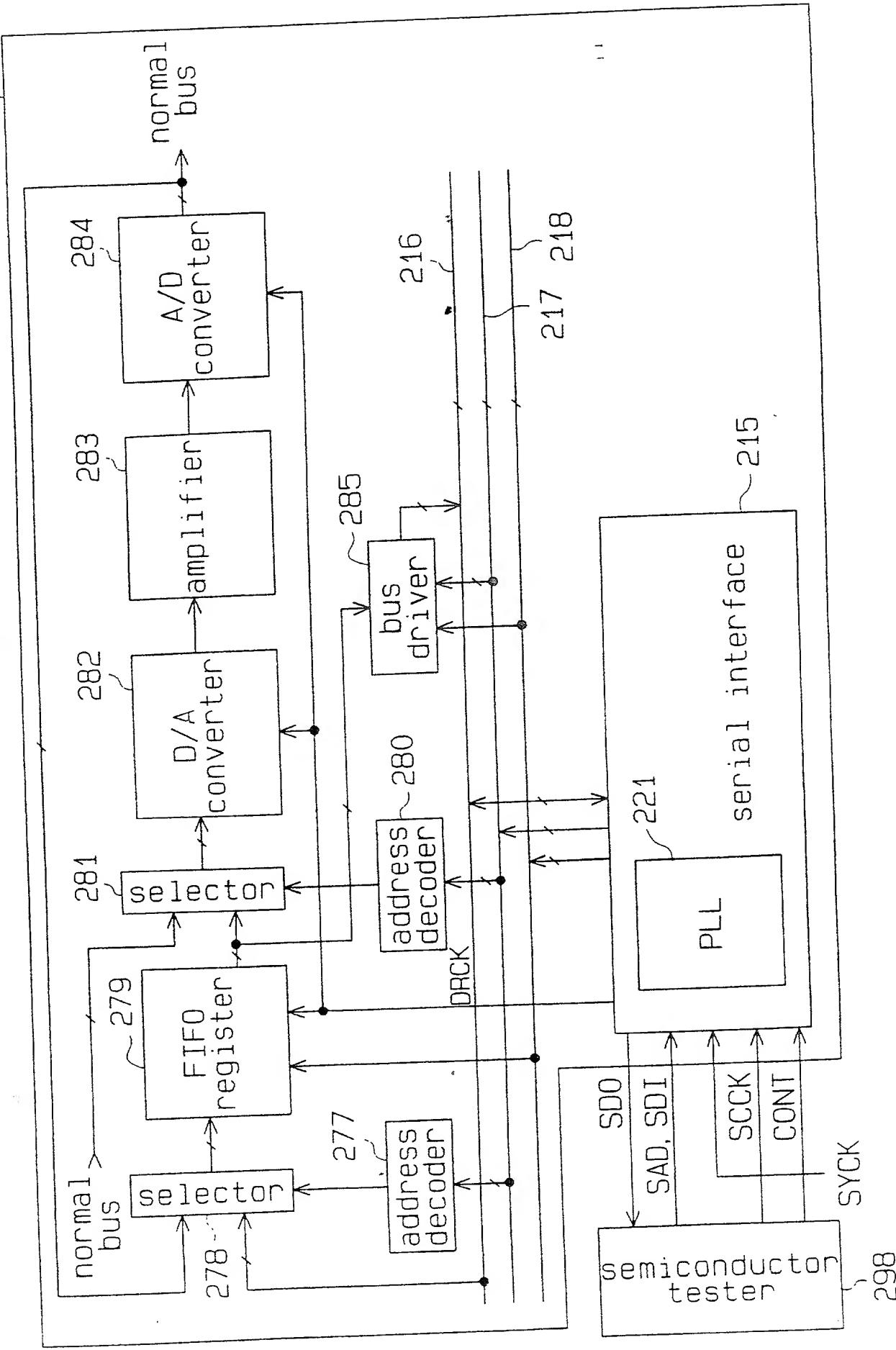
Fig. 16

Fig. 17

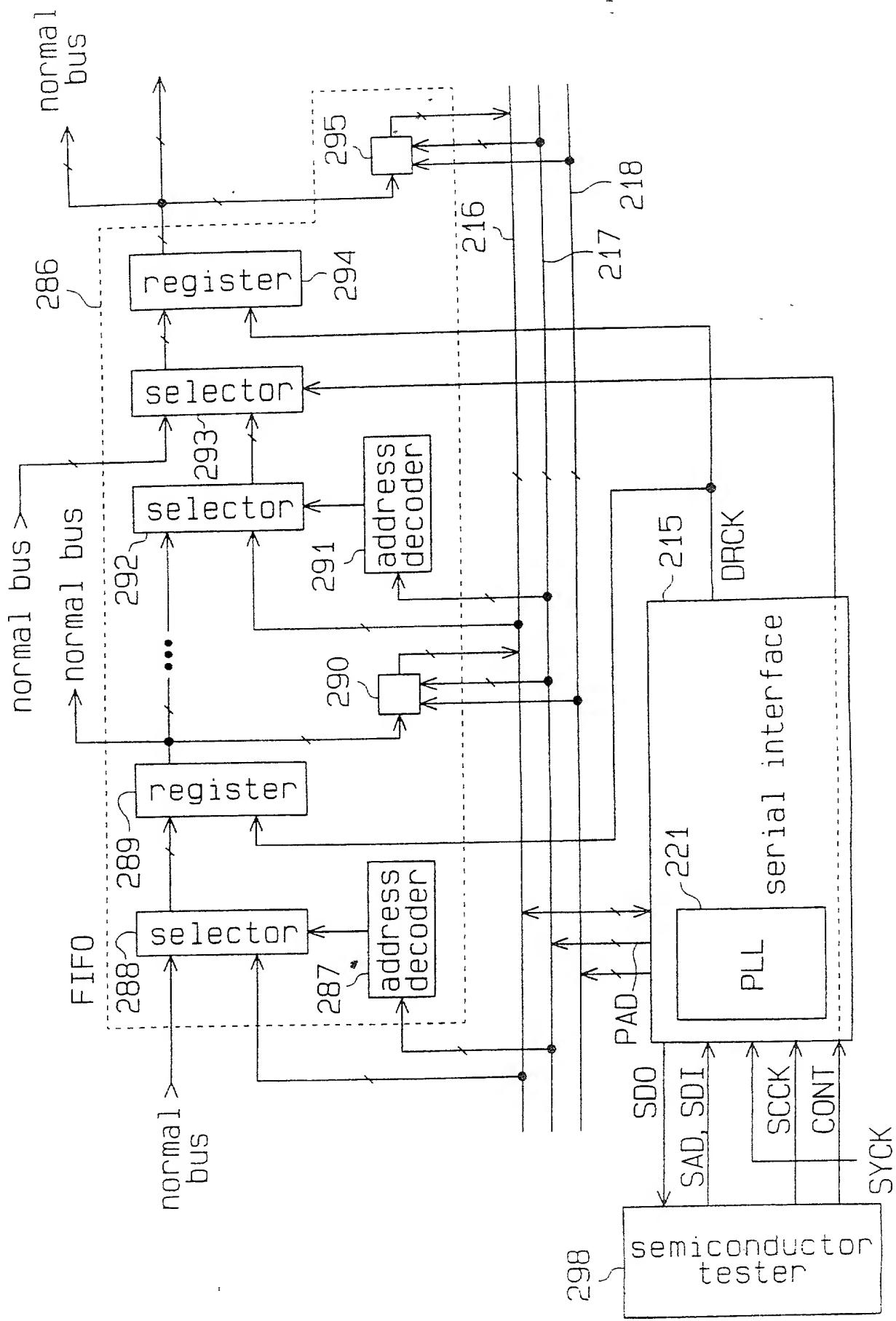


Fig. 18

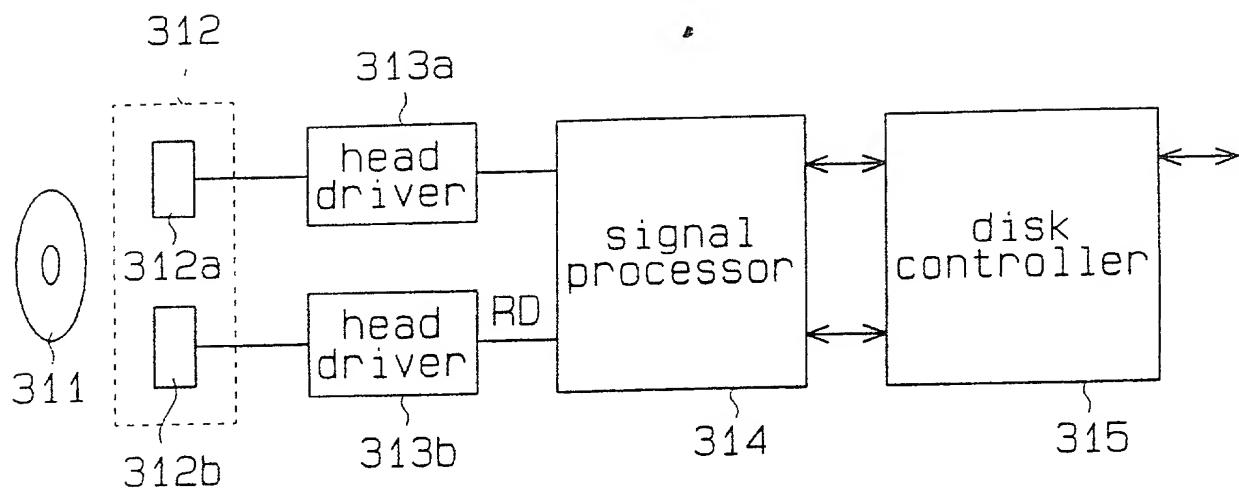


Fig. 19

read signal RD (analog)

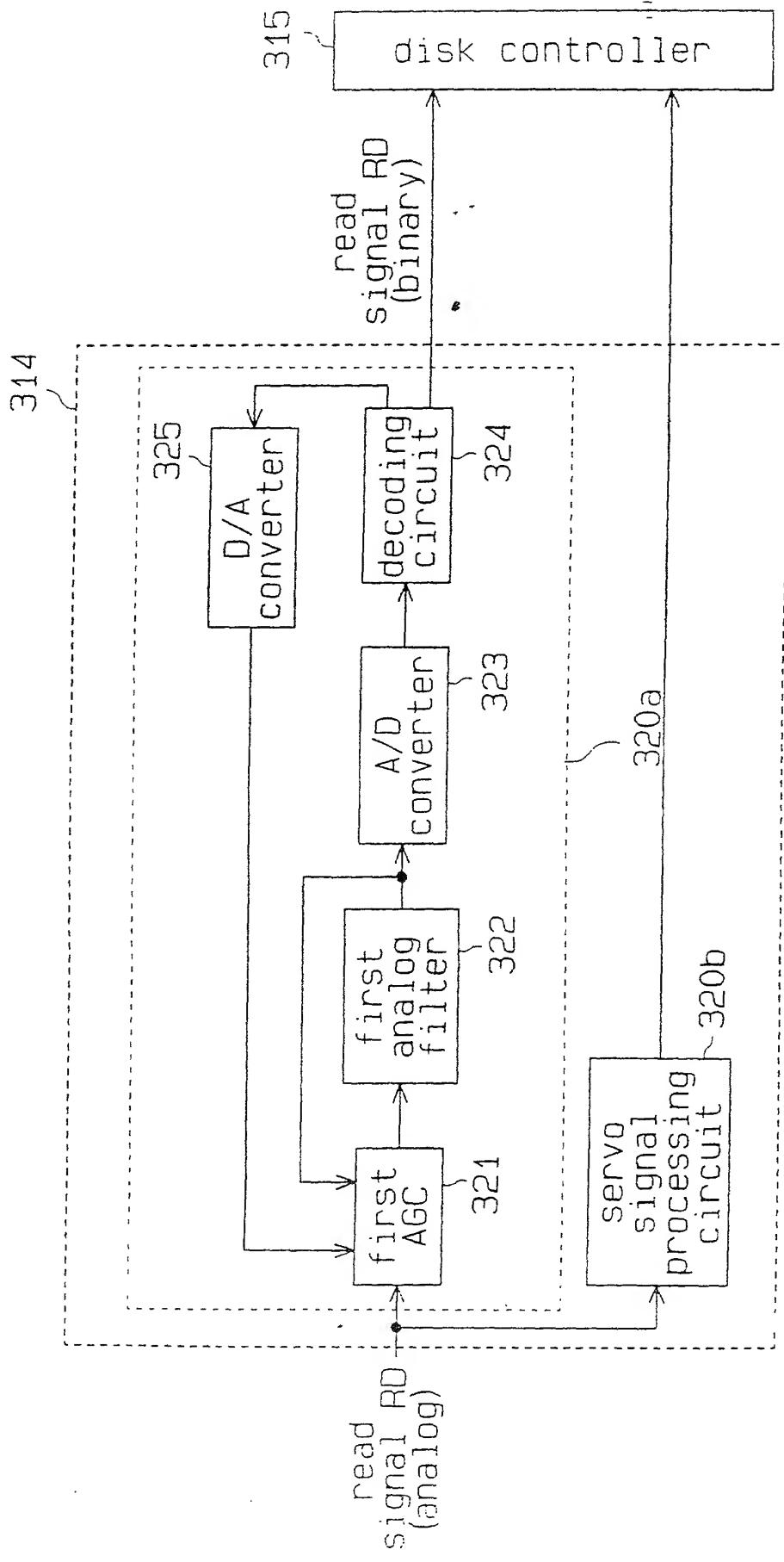


Fig. 20

Timing diagram of the read signal processing

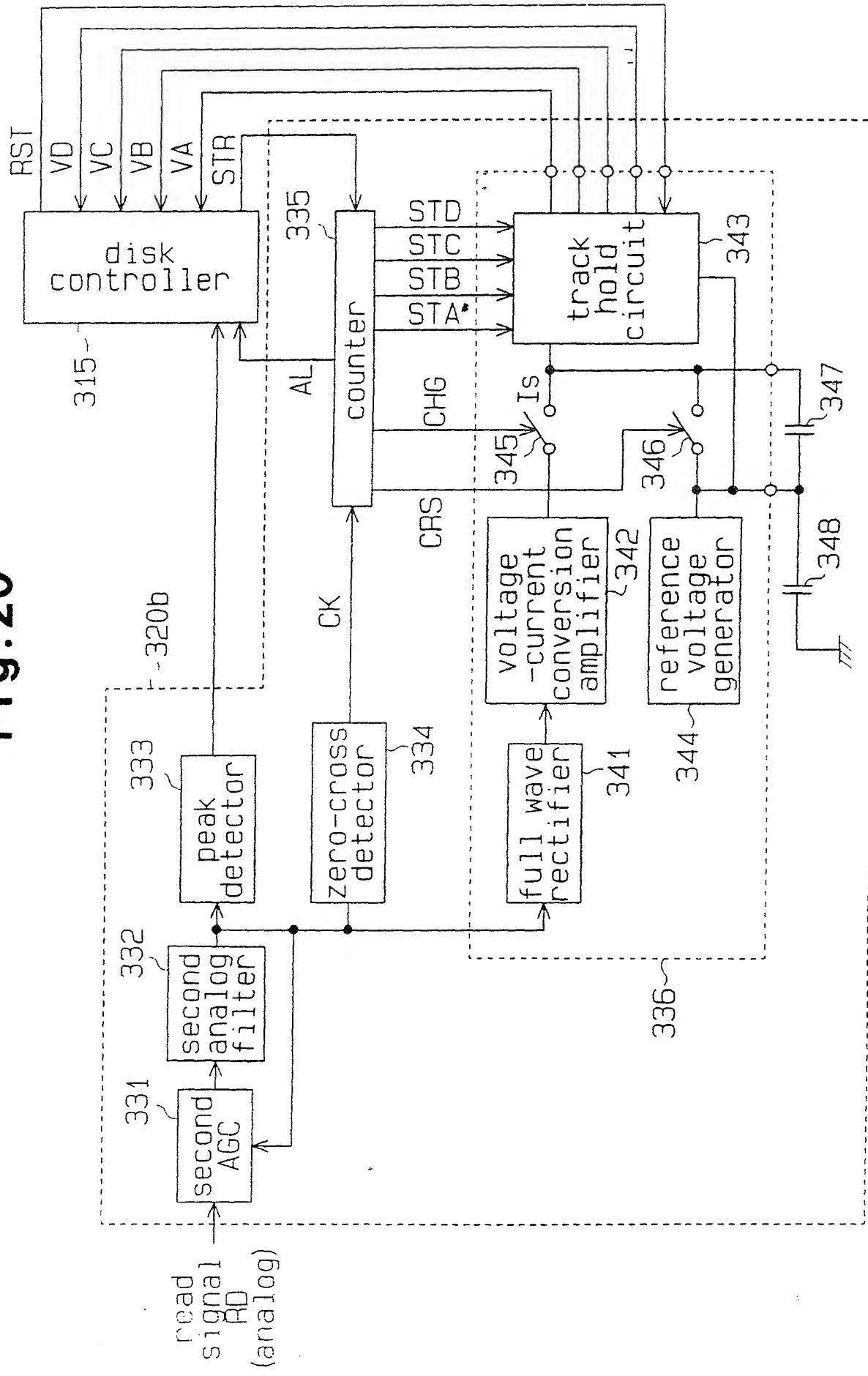


Fig. 21

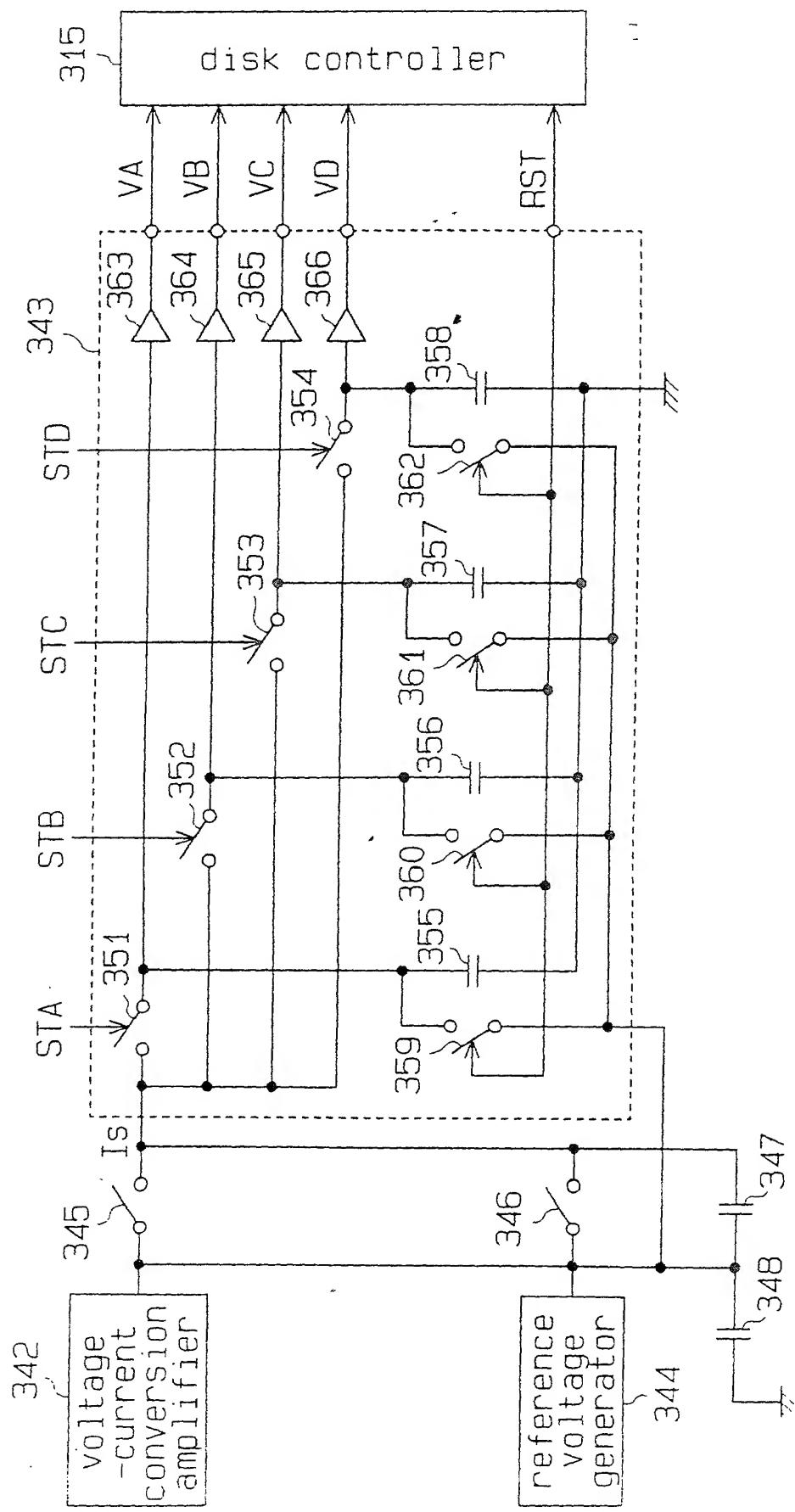


Fig.22

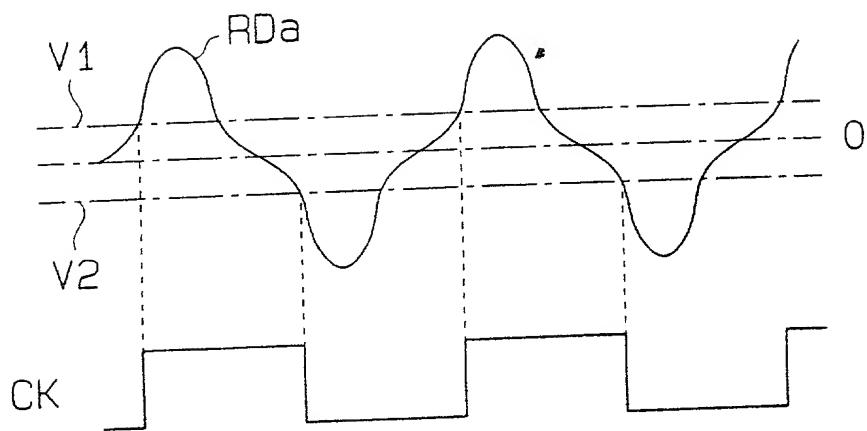


Fig. 23

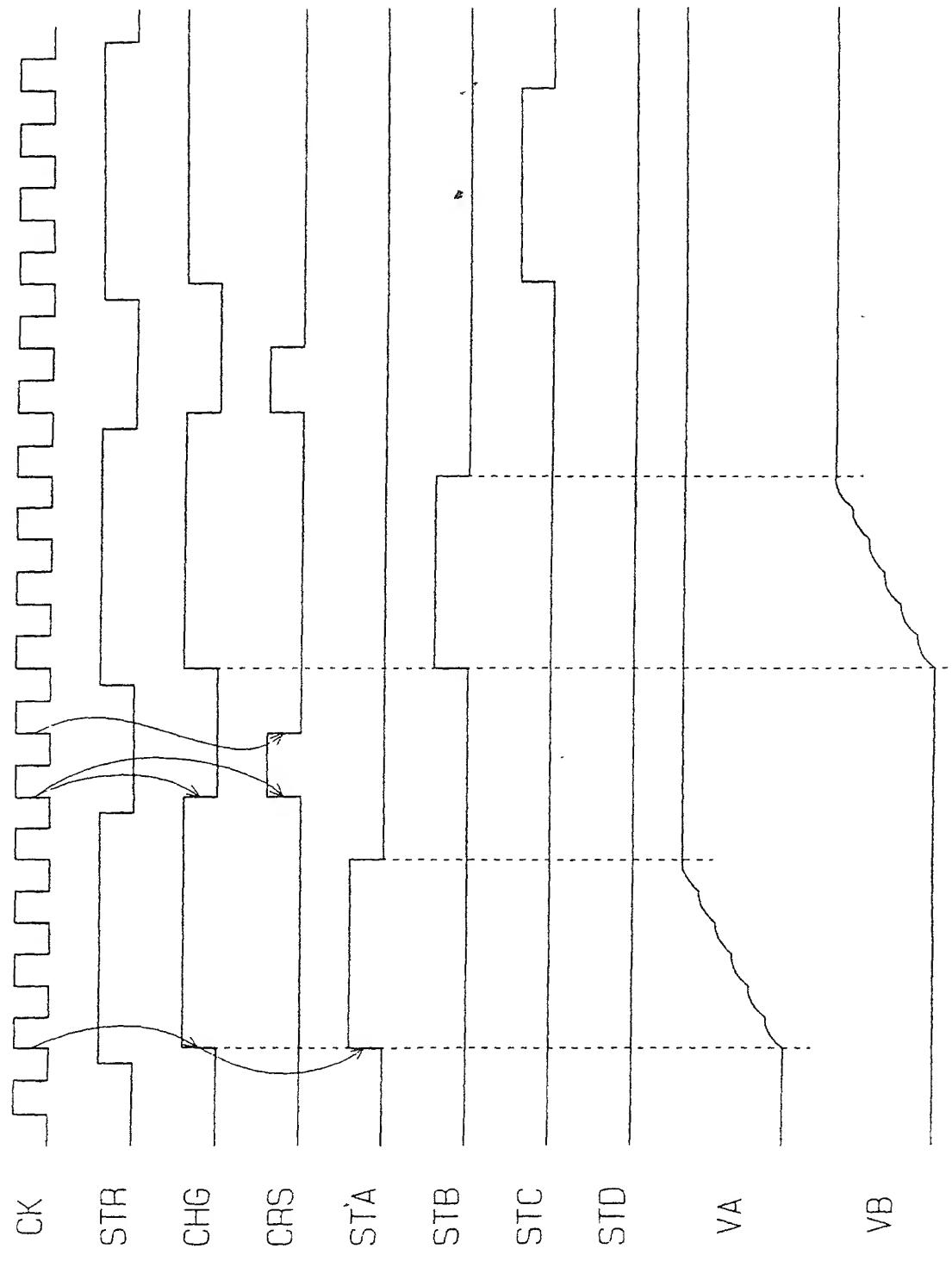


Fig. 24

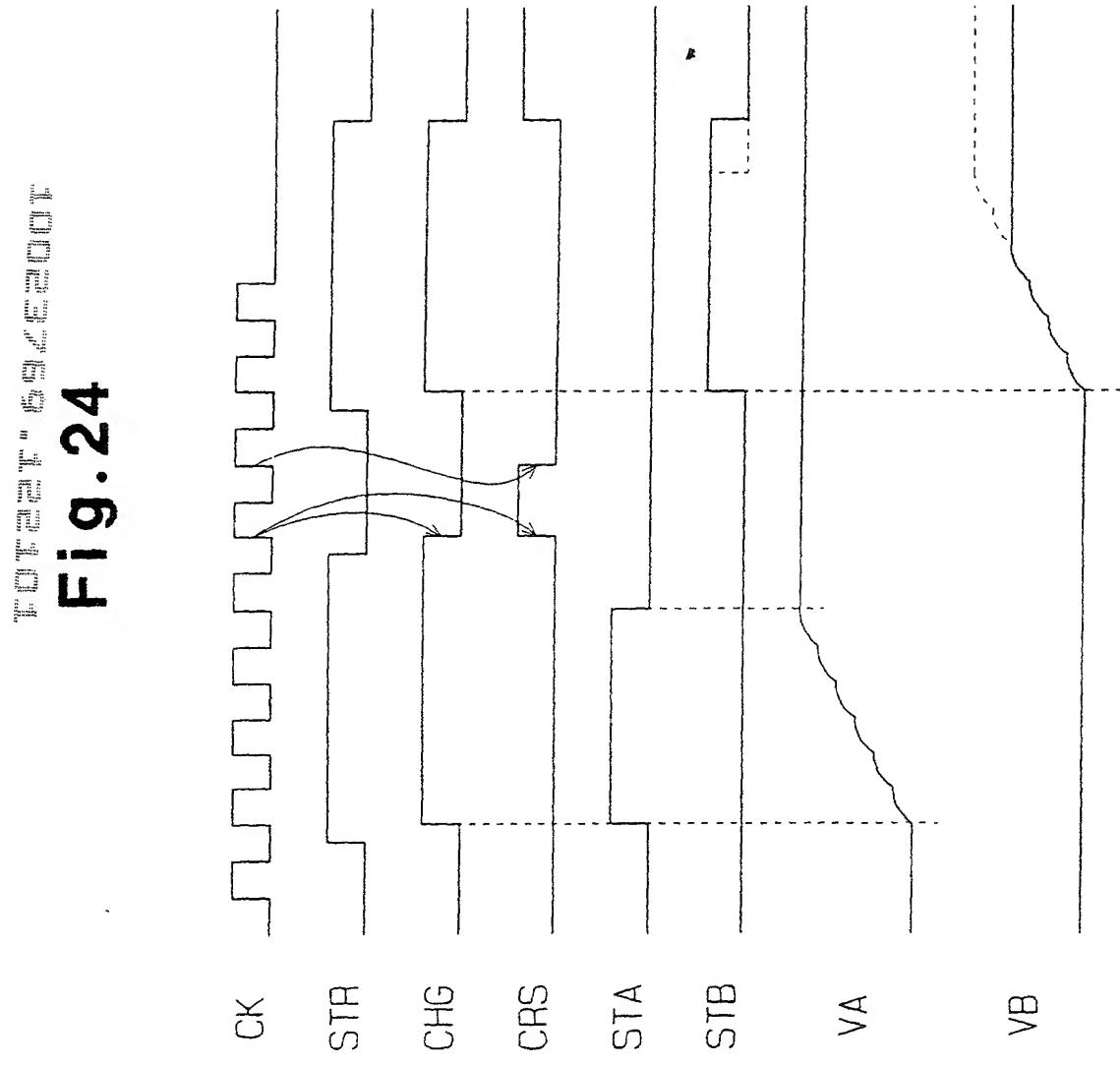


Fig. 25

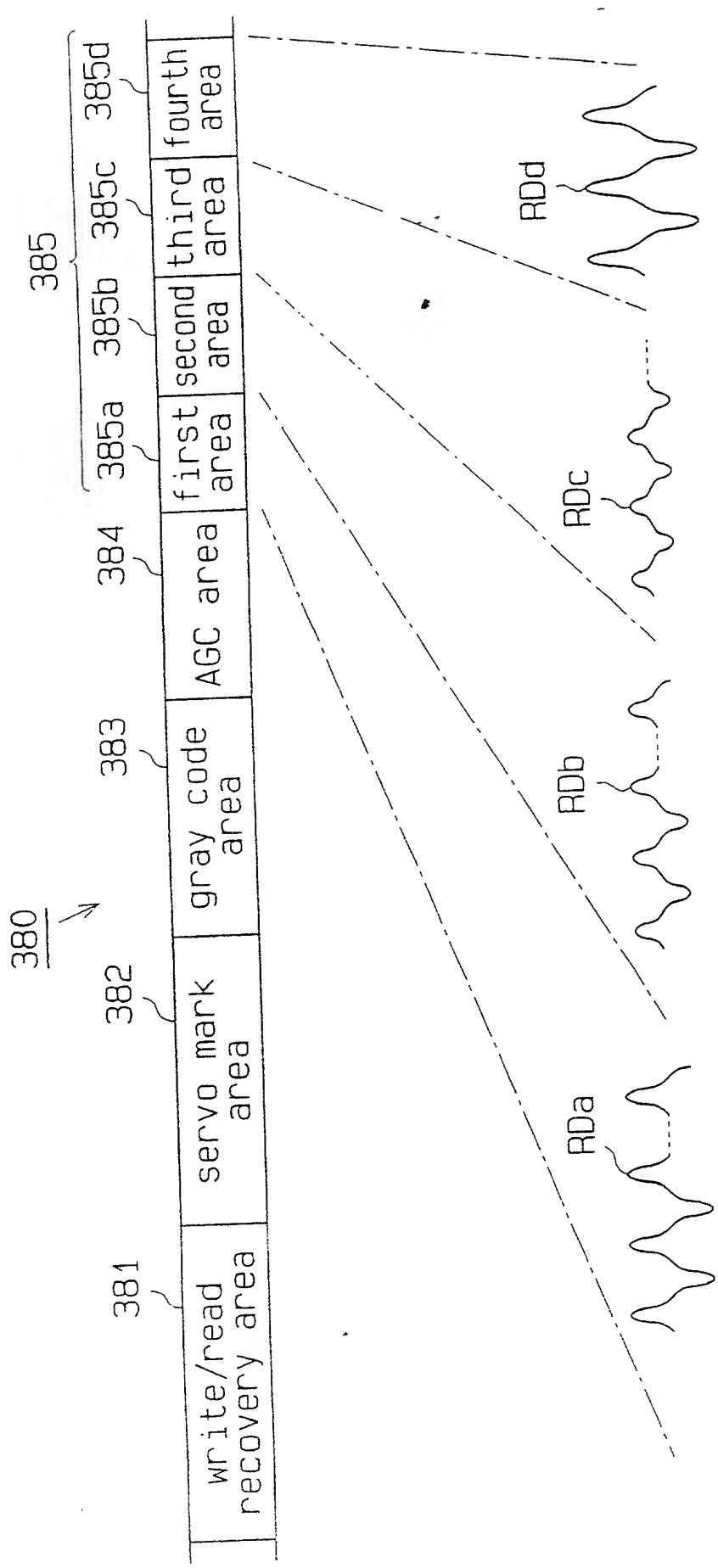


Fig. 26

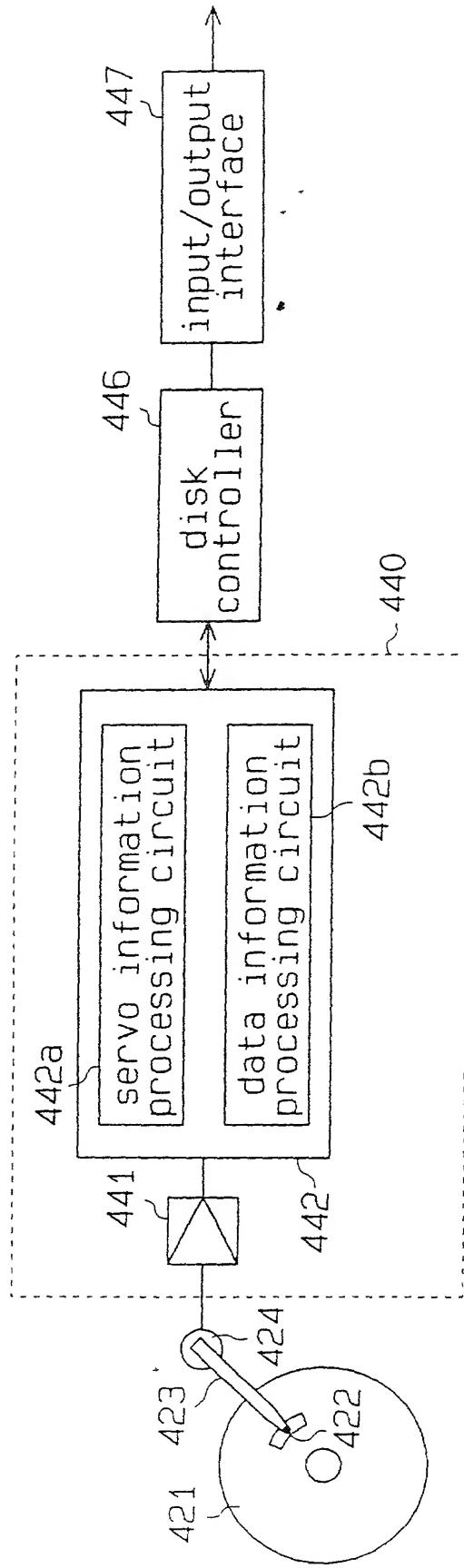


Fig. 27

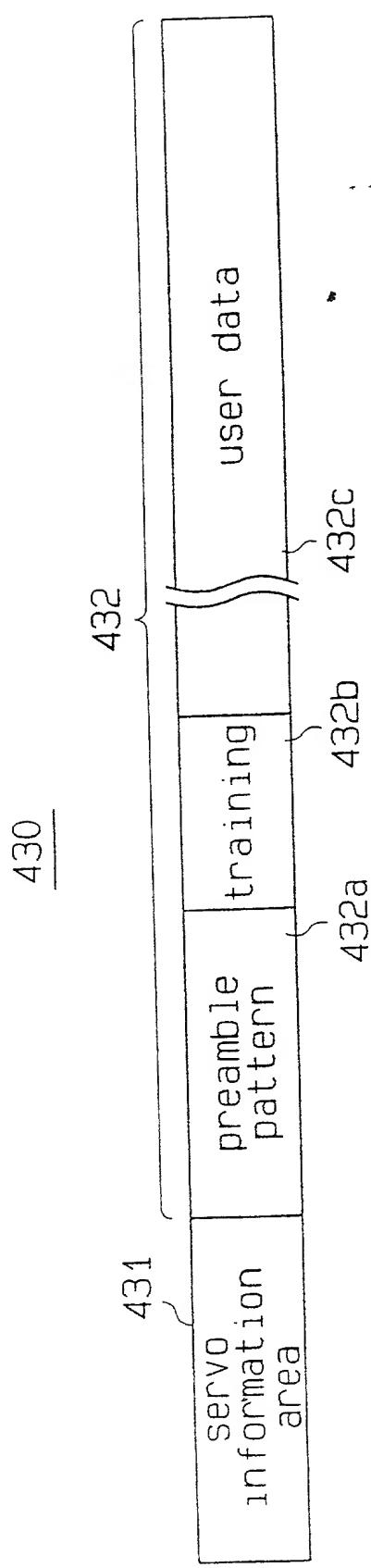


Fig. 28

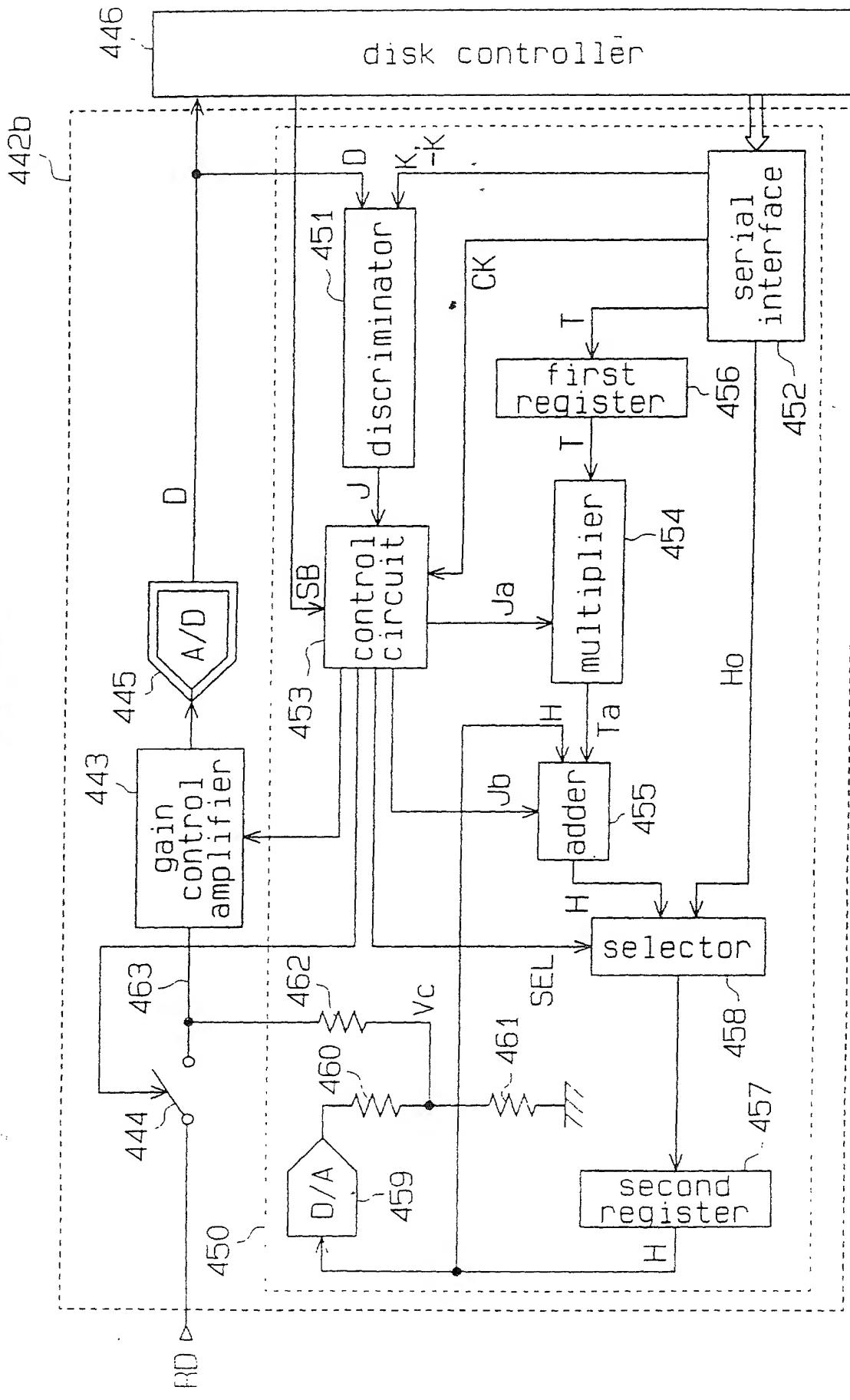


Fig. 29

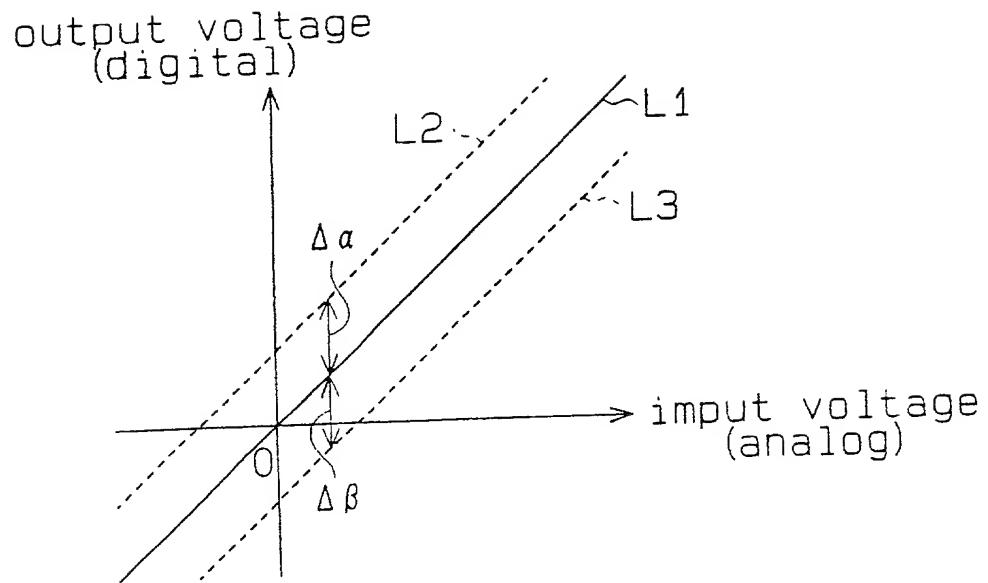


Fig. 30

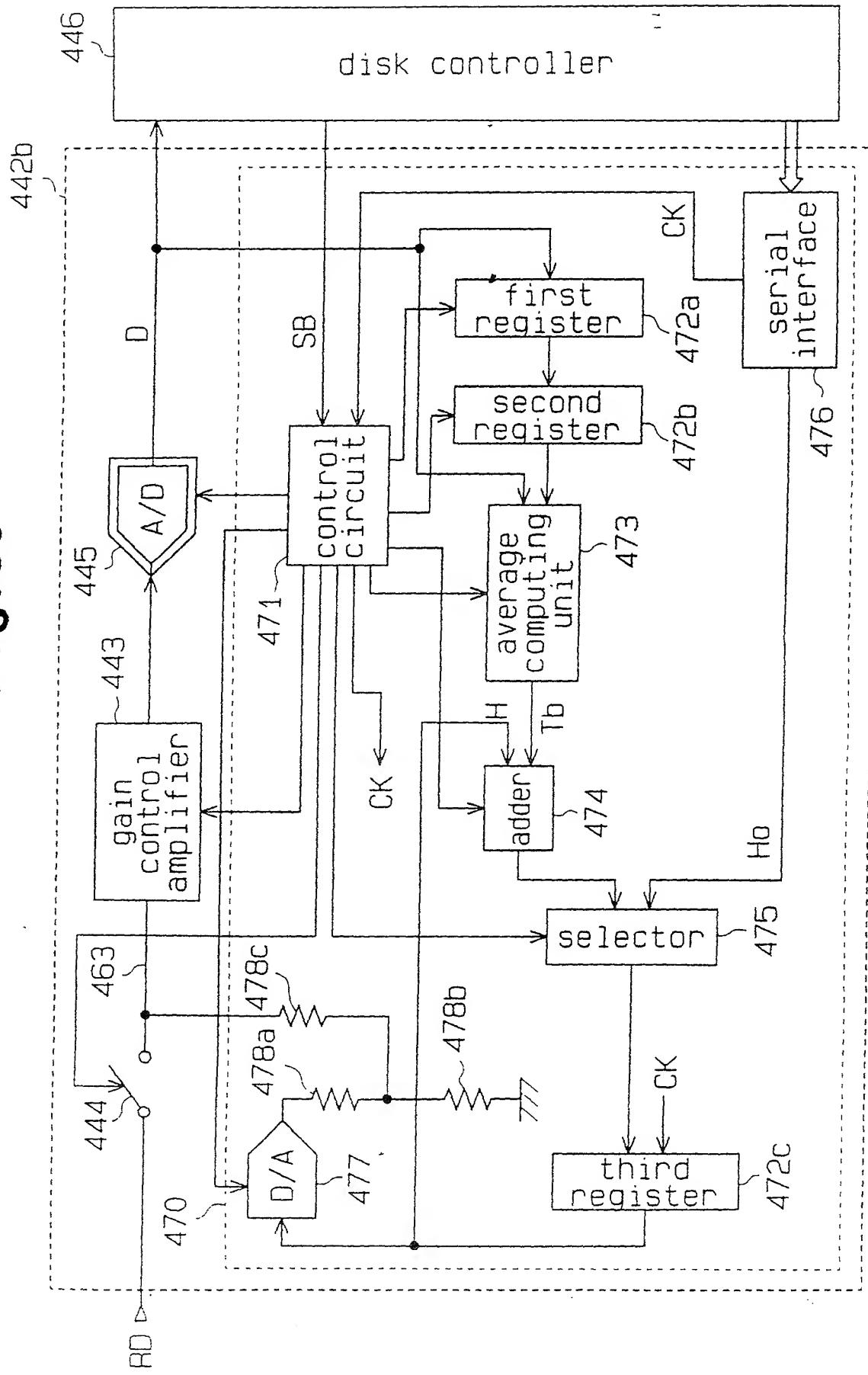


Fig. 31

MAX
0
MIN

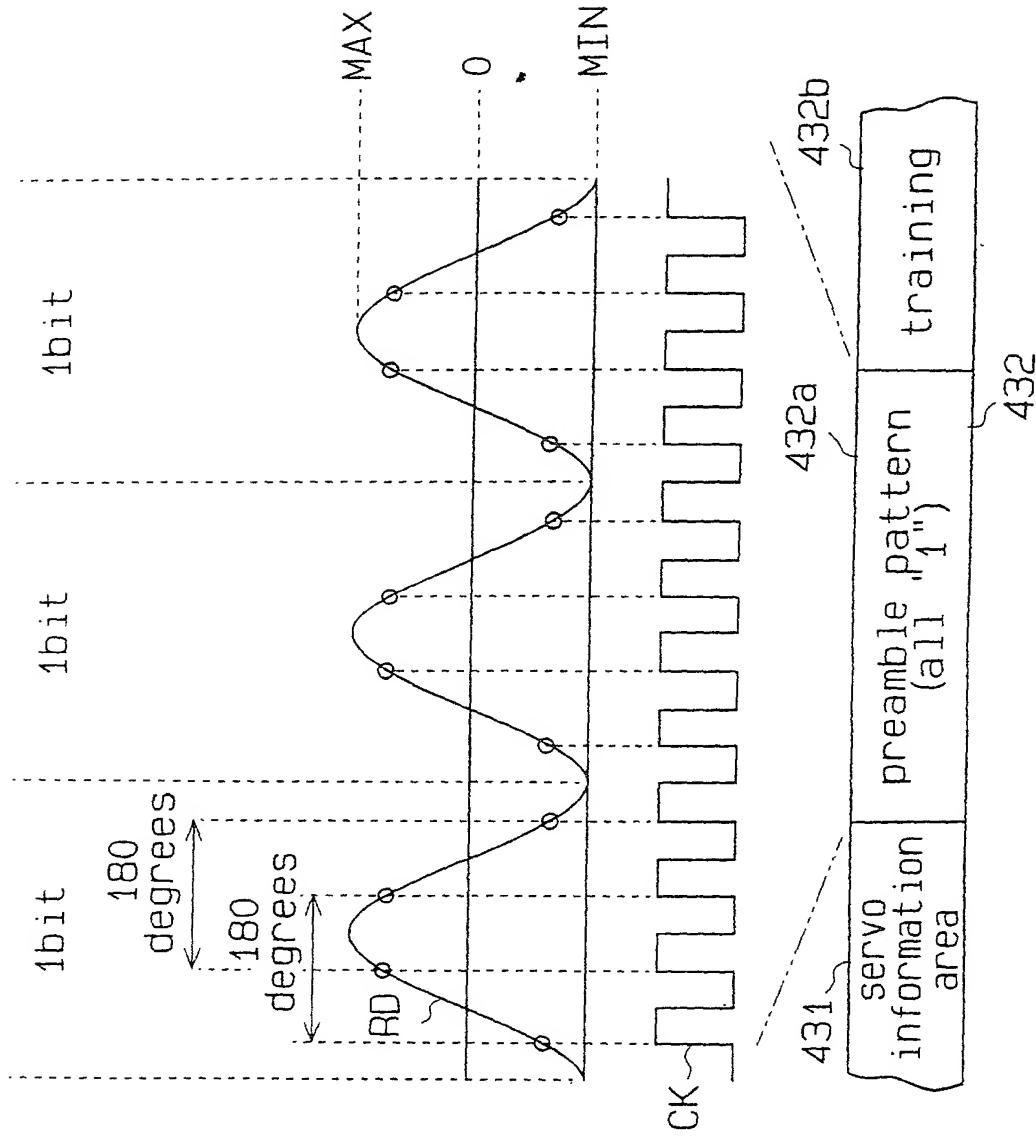


Fig. 32

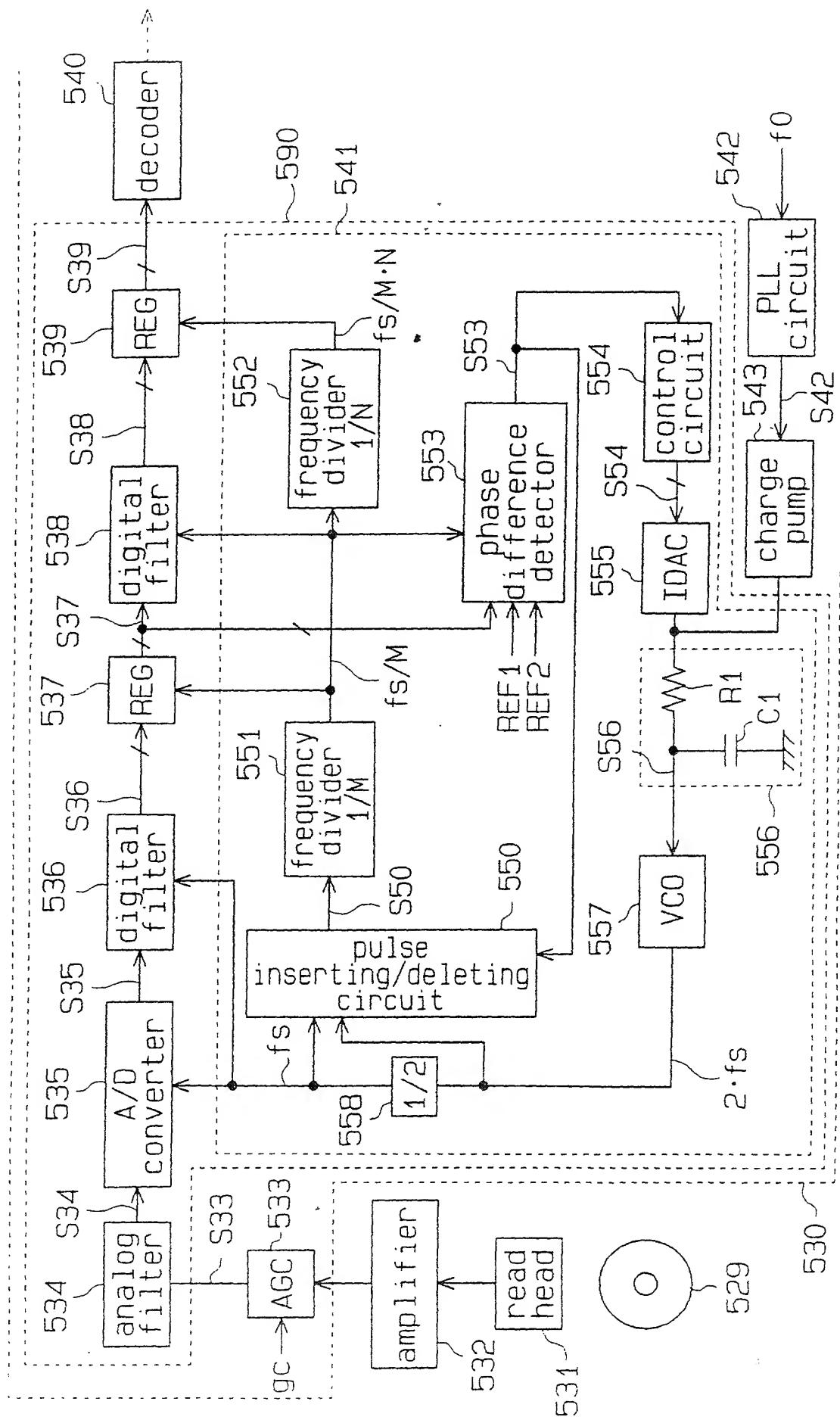


Fig. 33

REF 1
REF 2

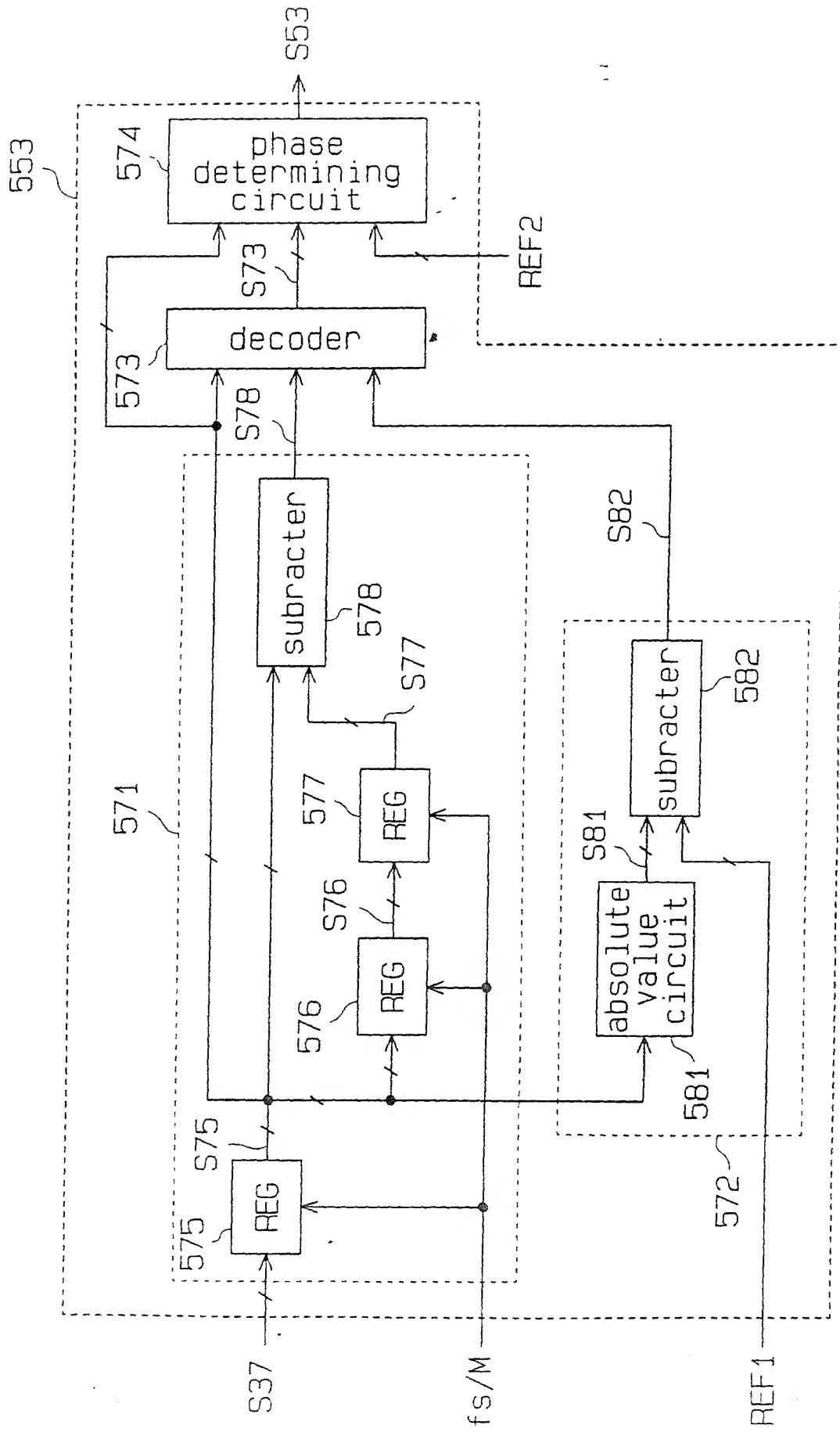


Fig.34A

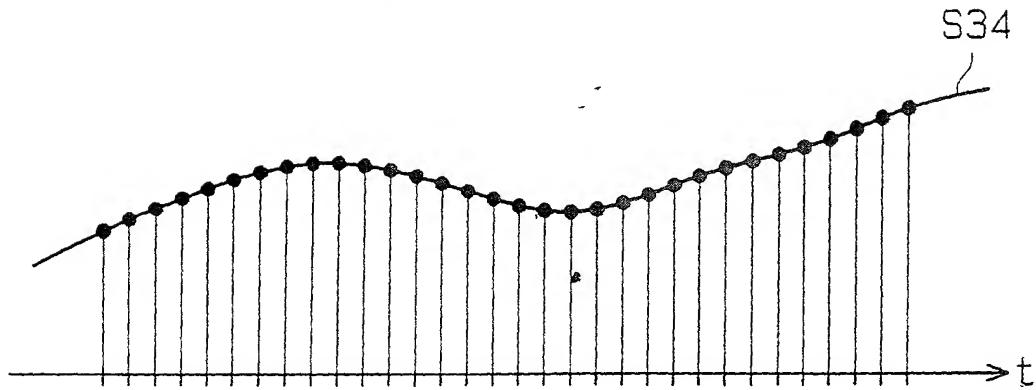


Fig.34B

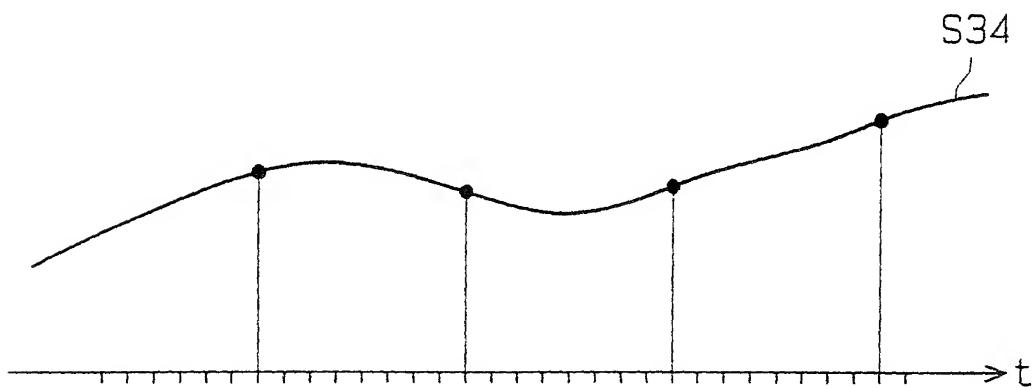


Fig.34C

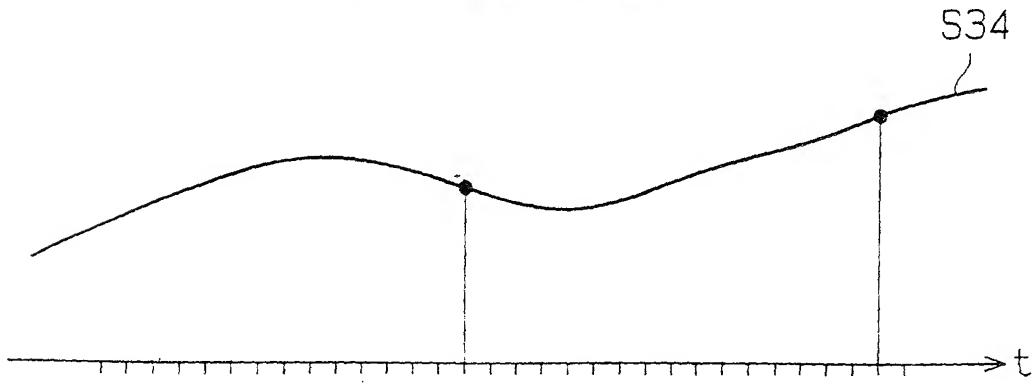


Fig. 35

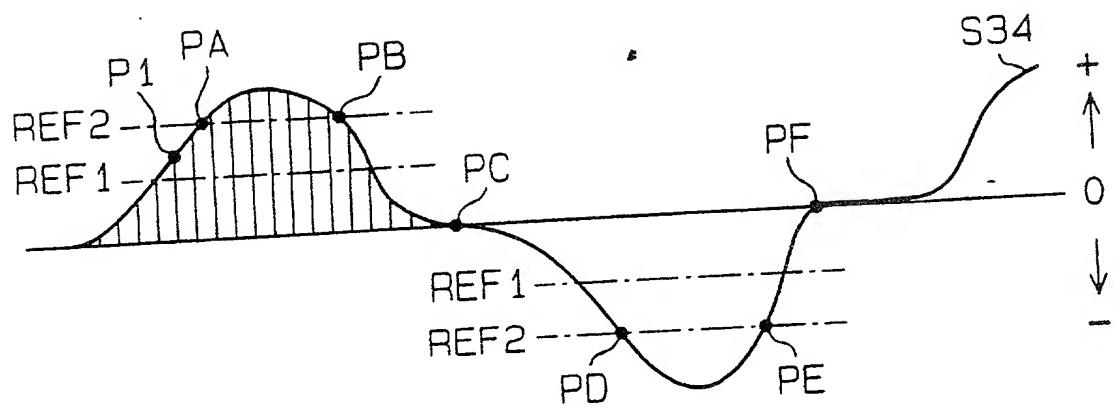


Fig. 36

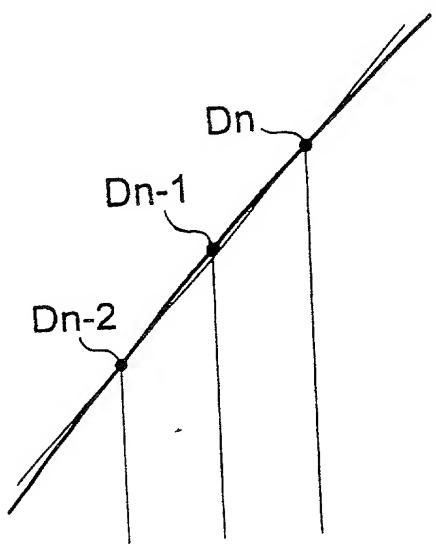


Fig.37

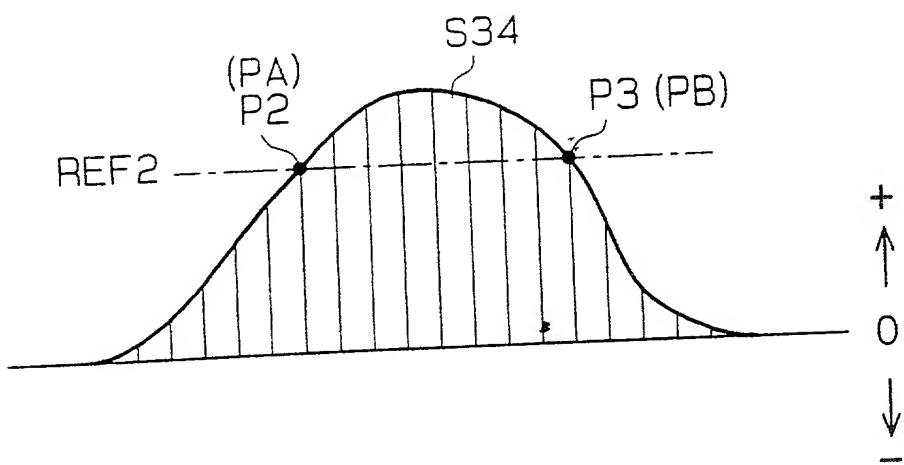


Fig.38

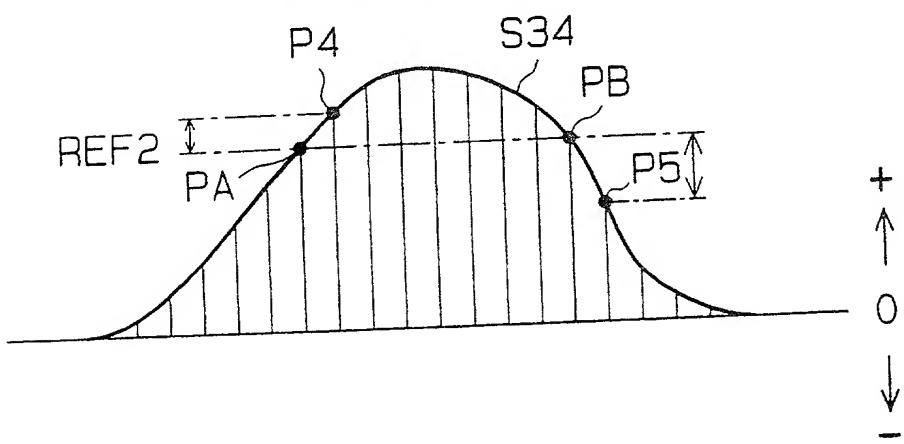
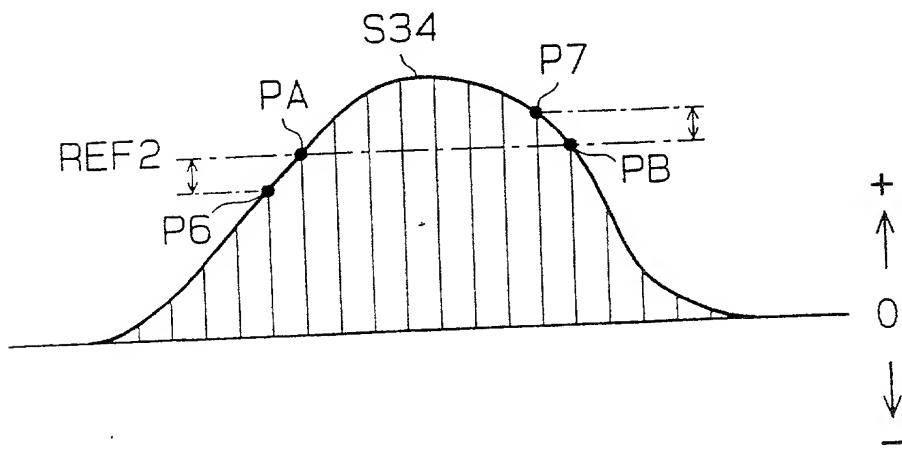


Fig.39



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Fig. 40A

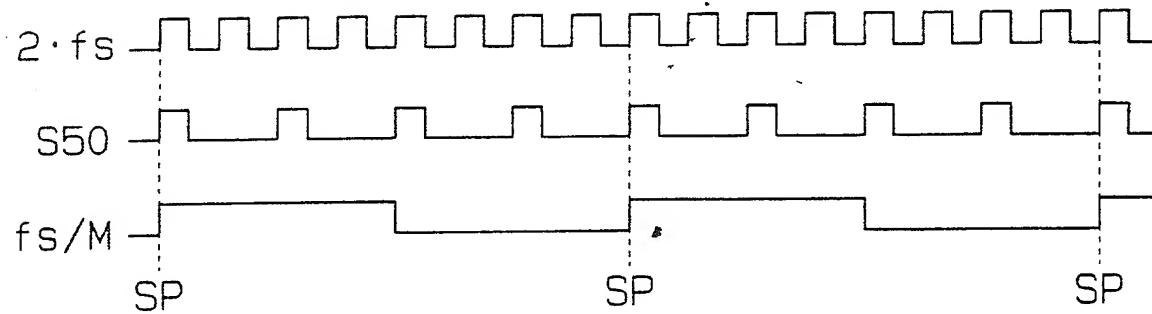


Fig. 40B

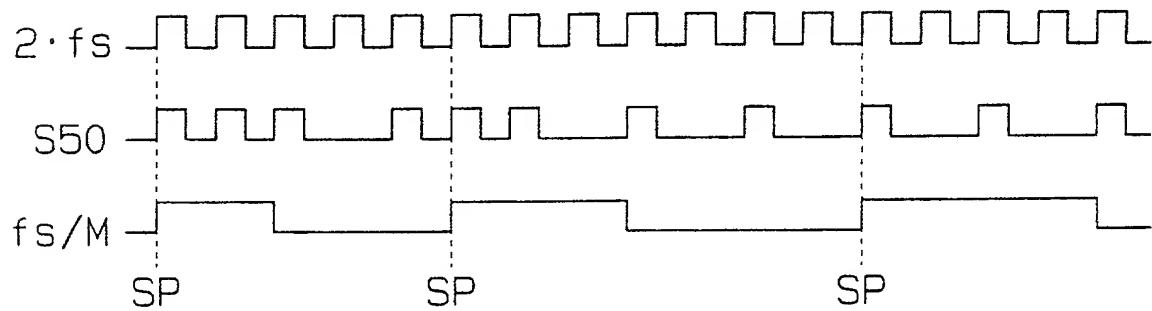


Fig. 40C

